UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 17-cv-05671-BLF

ORDER GRANTING IN PART AND DENYING IN PART VLSI'S MOTION FOR SUMMARY JUDGMENT; GRANTING IN PART AND DENYING IN PART INTEL'S MOTION FOR SUMMARY JUDGMENT

[Re: ECF Nos. 580, 586]

Plaintiff VLSI Technology LLC ("VLSI") brought the instant patent infringement action against Defendant Intel Corporation ("Intel"). At issue are four patents: U.S. Patent No. 8,566,836 ("'836 Patent"), U.S. Patent No. 8,004,922 ("'922 Patent"), U.S. Patent No. 7,675,806 ("'806 Patent"), and U.S. Patent No. 8,268,672 ("'672 Patent") (collectively the "Asserted Patents"). VLSI accuses various Intel technologies and processes of infringing the Asserted Patents.

Before the Court are the parties' Motions for Summary Judgment. VLSI seeks summary judgment (1) in VLSI's favor on Intel's affirmative defense that it is licensed to use all asserted patents and (2) of no invalidity based on six prior art combinations under IPR estoppel. ECF No. 586 ("VLSI Mot.") at 1, 15–16; ECF No. 735 ("VLSI Reply"). Intel opposes the motion. ECF No. 672 ("Intel Opp."). Intel seeks summary judgment (1) of no infringement of the '836 Patent, (2) of no infringement of the '922 Patent, (3) of invalidity of the asserted claims for the '922 Patent, (4) of no infringement of the '806 Patent, (5) of no infringement of the '672 Patent, (6) that it is licensed to use the Asserted Patents, and (7) of no willful infringement, no indirect infringement, and no enhanced damages for any patent. ECF No. 580 ("Intel Mot.") at 1; ECF No. 710 ("Intel Reply"). VLSI opposes the motion. ECF No. 677 ("VLSI Opp.").

After careful consideration, VLSI's Motion for Summary Judgment is GRANTED IN PART and DENIED IN PART and Intel's Motion for Summary Judgment is GRANTED IN PART and DENIED IN PART.

I. BACKGROUND

A. '836 Patent

The '836 Patent, entitled "Multi-Core System on Chip," claims a multi-core chip "in which a speed information for each core, such as the maximum operation speed" is extracted and stored, then "may be accessed and used by the operating system when allocating workload among the cores by selecting the fasted [sic] core to run any applications or tasks that can not be executed on a plurality of cores." '836 Patent at Abstract (cleaned up). More succinctly, when a single-core task is given to a multi-core processor, the processor gives that task to the fastest core. *See id.* at 2:1–13.

VLSI accuses Intel of infringing claims 1, 9–11, 13, 17, 20, and 21 of the '836 Patent. Each asserted claim requires, among other things, that "upon identifying" a task as a single-core task, the fastest core in the processor is "select[ed]" (claims 1, 9–11, 13, 17) or "identified" (claims 20, 21) to run that single-core task. ECF No. 241 ("Markman Order") 22–25 (construing claim 10 to include the same "upon identifying" limitation as claims 1 and 20).

B. '922 Patent

The '922 Patent, entitled "Power Island with Independent Power Characteristics for Memory and Logic," claims a power island with two segments, a first segment that "includes a hardware device and operates the hardware device at first power characteristics" and second segment that "includes scalable logic and operates the scalable logic at second power characteristics" such that the first and second power characteristics "are different." '922 Patent at Abstract.

VLSI accuses Intel of infringing claims 4, 5, and 18 of the '922 Patent. The Asserted Claims of the '922 Patent require certain components within the "power island" to have "power characteristics" that are "different" (claims 4 and 5) or "partially different" (claim 18) from the "power characteristics" of other components within the "power island." '922 Patent at 9:15–20,

12:6–13. The Asserted Claims also require a "supply power converter" that converts "external supply signal (VDD)" ('922 Patent at 9:27–37, 12:1–13) and a "reference power converter" that converts "reference signal (VSS)" ('922 Patent at 9:50–61, 12:23–28).

C. '806 Patent

The '806 Patent, entitled "Low Voltage Memory Device and Method Thereof," claims two memories, a "first memory" and a "second memory," both of which are located in an integrated circuit. '806 Patent at Abstract. "The first memory is a relatively high-density memory device, capable of storing large amounts of data relative to the second memory" and the "second memory is a low-voltage memory device capable of being accessed at low-voltages relative to the voltage at which the first memory can be accessed." *Id.* The circuit is thus "able to store large amounts of data in the high density memory in a normal or active mode of operation, and also have access to the low-voltage memory during the low-voltage mode of operation." *Id.*

VLSI accuses Intel of infringing claims 11, 12, 13, and 15 of the '806 Patent. The Asserted Claims require a "first memory" and a "second memory," and two different modes of operation: "a first mode of operation" and "a second mode of operation." '806 Patent at 10:31–57. The Court construed "second mode of operation" to require that, "when in the second mode of operation, both the voltage provided to the first memory and the voltage provided to the second memory must be lower than the minimum operating voltage of the first memory." Markman Order at 7.

D. '672 Patent

The '672 Patent, entitled "Method of Assembly and Assembly Thus Made," claims an assembly "comprising a first chip and a second chip which are interconnected through solder connections" that "comprise, at the first chip, an underbump metallization and a solder bump, and, at the second chip, a metallization" such that "the solder bump is provided as a fluid layer with a contact angle of less than 90°." '672 Patent at Abstract.

VLSI accuses Intel of infringing claim 2 of the '672 Patent. Claim 2 is directed to "[a] method of assembly of a first chip to a second chip" that includes a series of steps, including (1) "providing . . . a solder composition" to "a plurality of bond pads at a surface of the first chip . . .

with an underbump metallization," "wherein the solder composition is provided as a fluid layer on the underbump metallization," and (2) further requiring that the solder composition "makes a contact angle of less than 90° with the underbump metallization." '672 Patent at 8:2–22; Markman Order at 19.

E. License Agreement

In 2012, Intel entered into an agreement with certain Finjan entities and affiliates, whereby Intel received a "perpetual, irrevocable license" to "Finjan's Patents[.]" ECF No. 579-17 ("Finjan License Agreement" or "Agreement") § 3.1. The term "Finjan" expressly includes Finjan, Inc., Finjan Software, Inc., and their "Affiliates." *Id.* at Preamble. The term "Affiliates" is defined as "any Person that, now or hereafter, directly or indirectly through one or more entities, controls or is controlled by, or is under common control with, [a] specified Person." *Id.* §1.2. Fortress Investment Group ("Fortress"), the company that formed and controls VLSI, acquired control of Finjan Holdings LLC ("FHL") in 2020. Intel Mot. at 18.

VLSI and its parent company CF VLSI Holdings LLC ("VLSI Holdings") were created in 2016 for the purpose of acquiring and licensing a portfolio of semiconductor patents from NXP Semiconductors ("NXP"). VLSI Mot. at 2. VLSI and VLSI Holdings were capitalized by ten different investment funds managed by Fortress, with the majority investor in VLSI Holdings being Fortress Credit Opportunities Fund IV ("FCO IV"), which is a closed-end mutual fund with hundreds of investors and $1.8 billion under management as of June 30, 2022. ECF No. 586-3 ("LLC Agreement") at VLSI-18-966DE00050646; ECF No. 586-4 ("Stolarski Decl.") ¶¶ 7, 10; ECF No. 589-2 (Zur Dep.) 119:10–25; ECF No. 589-3 (James Dep.) 131:19–132:6; ECF No. 586-7 (2022-07-11 Del. Stolarski Decl.) ¶ 5. VLSI is 100% owned by VLSI Holdings, which in turn is owned by 10 different investment funds (with the majority owner being FCO IV), all of which are managed by Fortress. LLC Agreement at VLSI-18-966DE00050646; Stolarski Decl. ¶ 10.

VLSI and NXP entered into a Patent Purchase and Cooperation Agreement ("PPCA"), by which VLSI purchased a group of semiconductor patents that had been developed by NXP and its predecessors, and NXP agreed to cooperate in VLSI's assertion of the NXP patents against Intel and others. In exchange, NXP received a large upfront payment from VLSI and is entitled to a

share of licensing profits that VLSI obtains on the NXP patents. Stolarski Decl. ¶ 4; ECF No. 586-9 (Stolarski Dep. 10/17/19) 227:24–228:20; ECF No. 586-10 (Stolarski Dep. 7/9/20) 146:12–14, 148:22–149:3; ECF No. 586-11 (PPCA) at §§ 2.1, 7.3.

F. Procedural History and Parallel Litigation

In October 2017, VLSI filed this action against Intel asserting several of the NXP patents. ECF No. 1 ("Compl."). VLSI subsequently filed a separate patent infringement action against Intel on other NXP patents in the District of Delaware, as well as three more patent infringement actions against Intel on NXP patents in the Western District of Texas. VLSI Mot. at 3. The later four district court actions initiated by VLSI against Intel have already been largely resolved at the trial court level: the first Western District of Texas case resulted in a $2.18 billion jury verdict and subsequent judgment in favor of VLSI, which the Federal Circuit has recently reversed; the second Western District of Texas case resulted in a defense verdict for Intel; the third Western District of Texas case resulted in a $949 million jury verdict in favor of VLSI that is presently at the post-trial motion stage; and the Delaware suit was dismissed on December 27, 2022 by mutual agreement of the parties before any trial date had been set. *Id.*

Intel first asserted its license defense against VLSI on September 2, 2020 in one of the Western District of Texas actions (*VLSI Technology LLC v. Intel Corporation*, No. 6:21-CV-57-ADA (W.D. Tex.)), and subsequently asserted the same license theory in the parties' District of Delaware action on September 11, 2020 (*VLSI Technology LLC v. Intel Corporation*, No. 18-cv-966-CFC-CJB (D. Del.)), in Delaware Chancery Court on January 11, 2021, and finally in this Court on December 15, 2021 (ECF No. 330-1 at 13). VLSI Mot. at 4.

II. LEGAL STANDARD

Federal Rule of Civil Procedure 56 governs motions for summary judgment. Summary judgment is appropriate if the evidence and all reasonable inferences in the light most favorable to the nonmoving party "show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law." *Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1986). The current version of Rule 56 authorizes a court to grant "partial summary judgment" to dispose of less than the entire case and even just portions of a claim or defense. *See*

Fed. R. Civ. Proc. advisory committee's note, 2010 amendments; *Ochoa v. McDonald's Corp.*, 133 F.Supp.3d 1228, 1232 (N.D. Cal. 2015).

The moving party "bears the burden of showing there is no material factual dispute," *Hill v. R+L Carriers, Inc.*, 690 F.Supp.2d 1001, 1004 (N.D. Cal. 2010), by "identifying for the court the portions of the materials on file that it believes demonstrate the absence of any genuine issue of material fact." T.*W. Elec. Serv. Inc. v. Pac. Elec. Contractors Ass'n*, 809 F.2d 626, 630 (9th Cir. 1987). In judging evidence at the summary judgment stage, the Court "does not assess credibility or weigh the evidence, but simply determines whether there is a genuine factual issue for trial." *House v. Bell*, 547 U.S. 518, 559–60 (2006). A fact is "material" if it "might affect the outcome of the suit under the governing law," and a dispute as to a material fact is "genuine" if there is sufficient evidence for a reasonable trier of fact to decide in favor of the nonmoving party. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986).

Where the moving party will have the burden of proof on an issue at trial, it must affirmatively demonstrate that no reasonable trier of fact could find other than for the moving party. *Celotex*, 477 U.S. at 325; *Soremekun v. Thrifty Payless, Inc.*, 509 F.3d 978, 984 (9th Cir. 2007). By contrast, where the moving party does not have the burden of proof on an issue at trial, it "must either produce evidence negating an essential element of the nonmoving party's claim or defense or show that the nonmoving party does not have enough evidence of an essential element to carry its ultimate burden of persuasion at trial." *Nissan Fire & Marine Ins. Co. v. Fritz Companies, Inc.*, 210 F.3d 1099, 1102 (9th Cir. 2000).

Once the moving party meets its initial burden, the nonmoving party must set forth, by affidavit or as otherwise provided in Rule 56, "specific facts showing that there is a genuine issue for trial." *Liberty Lobby*, 477 U.S. at 250 (internal quotation marks omitted). In determining whether a genuine issue of material fact exists, "[t]he evidence of the non-movant is to be believed, and all justifiable inferences are to be drawn in his favor." *Id.* at 255 (citation omitted). If the nonmoving party's "evidence is merely colorable, or is not significantly probative, summary judgment may be granted." *Id.* at 249–50 (internal citations omitted). Mere conclusory, speculative testimony in affidavits and moving papers is also insufficient to raise genuine issues of

fact and defeat summary judgment. *See Thornhill Publ'g Co. v. GTE Corp.*, 594 F.2d 730, 738 (9th Cir. 1979). For a court to find that a genuine dispute of material fact exists, "there must be enough doubt for a reasonable trier of fact to find for the [non-moving party]." *Corales v. Bennett*, 567 F.3d 554, 562 (9th Cir. 2009).

III. DISCUSSION

A. VLSI's Motion

1. License Defense

a. Res Judicata and Collateral Estoppel

VLSI had a strong argument that res judicata and collateral estoppel barred Intel's license defense until December 4, 2023 when the Federal Circuit reversed the Texas district court ruling on which this argument was based. *VLSI Technology LLC v. Intel Corporation*, Case No. 22-1906 (Fed. Cir. Dec. 4, 2023). With this turn of events, VLSI's motion on this ground is denied.

b. Merits of the License Defense

VLSI seeks summary judgment that it is not bound by the Finjan License Agreement. VLSI argues that it is not a party to the Agreement (VLSI Mot. at 7–12) and the Asserted Patents are not "Finjan's Patents" (*id.* at 12–15). The recency of the Federal Circuit's decision requires this Court to fully analyze the issues raised in the parties' Motions for Summary Judgment, which will require consideration of the Federal Circuit's ruling. In the interest of providing the parties with the bulk of its ruling on the motions without further delay, the Court will issue a supplemental order addressing the merits of the license defense as soon as possible.

2. IPR Estoppel

Next, VLSI seeks summary judgment of no invalidity based on six prior art combinations discussed in Intel's expert reports under the doctrine of IPR estoppel. Intel expert Dr. Alyssa B. Apsel's obviousness analysis concerns the'922 Patent, setting forth the following three combinations of prior art references:

(1) The Nehalem Processor ("Nehalem" or "Nehalem Processor"), U.S. Patent No. 8,397,090 ("Gunther"), and U.S. Patent No. 7,723,867 ("Willingham") (collectively, "Nehalem, Gunther, and Willingham") (ECF No. 588-7 ("Apsel Report") ¶¶ 771–961);

(2) U.S. Patent No. 8,171,323 ("Rakshani") and Willingham (collectively, "Rakshani and Willingham") (*id.* ¶¶ 962–1096);

(3) Rakshani and U.S. Patent No. 7,307,899 ("Khellah") (collectively, "Rakshani and Khellah") (*id.* ¶¶ 1097–1132).

VLSI Mot. at 17. Intel expert Dr. Patrick Fay's obviousness analysis concerns the '672 Patent, setting forth the following three combinations of prior art references:

(4) Japanese Patent Application JP-A 02-005455 ("Okada"), U.S. Patent No. 6,070,788 ("Zakel"), and the Lee Book (collectively, "Okada, Zakel, and the Lee Book") (ECF No. 588-8 ("Fay Report") ¶¶ 139–88);

(5) Okada, the Lee Book, and the Intel P1264 Package Process ("P1264 Process") (collectively, "Okada, the Lee Book, and the Intel P1264 Package Process") (*id.* ¶¶ 189–246); and

(6) Barbara Pahl et al., *A Thermode Bonding Process for Fine Pitch Flip Chip Applications Down to 40 Micron*, 2001 Proceedings, Int'l Symp. on Elec. Materials & Packaging ("Pahl"), U.S. Patent Application Publication No. 2002/0149117 ("Shibata"), and U.S. Patent Application Publication No. 2004/0012090 ("Basol") (collectively, "Pahl, Shibata, and Basol") (*id.* ¶¶ 247–86).

VLSI Mot. at 17. VLSI seeks summary judgment that Intel should be estopped from asserting these six obviousness combinations.

A petitioner whose challenge to a patent claim in IPR results in a Final Written Decision cannot later assert in litigation "that the claim is invalid on any ground that the petitioner . . . reasonably could have raised during that inter partes review." 35 U.S.C. § 315(e)(2). "[E]stoppel applies not just to claims and grounds asserted in the petition and instituted for consideration by the Board, but to all grounds not stated in the petition but which reasonably could have been asserted against the claims included in the petition." *Click-to-Call Techs. LP v. Ingenio, Inc.*, 45 F.4th 1363, 1370 (Fed. Cir. 2022) (quoting *California Inst. of Tech. v. Broadcom Ltd.*, 25 F.4th 976, 991 (Fed. Cir. 2022)).

VLSI makes three arguments. First VLSI argues that three of the combinations – (2)

Rakshani and Willingham; (3) Rakshani and Khellah; and (6) Pahl, Shibata, and Basol – are barred because each of the references was disclosed before or as part of Intel's IPR Petitions. VLSI Mot. at 17–19. Second, VLSI argues that the combination (4) Okada, Zakel, and the Lee Book is barred because it relies on the Lee Book. *Id.* at 19–20. Third, VLSI argues that two of the combinations – (1) Nehalem, Gunther, and Willingham; and (5) Okada, the Lee Book, and the Intel P1264 Package Process – are barred because they improperly rely on "product" prior art. *Id.* at 20–25.

a. Prior Art Disclosed by June 2018

First, VLSI seeks summary judgment that IPR Estoppel bars Intel from three obviousness combinations: (2) Rakshani and Willingham; (3) Rakshani and Khellah; and (6) Pahl, Shibata, and Basol. VLSI lists several asserted prior art references Dr. Apsel and Dr. Fay rely on for their Section 103 obviousness analyses that Intel disclosed in its March 19, 2018 Invalidity Contentions and June 2018 IPR petitions. VLSI Mot. at 18. VLSI presents evidence that Intel disclosed Rakshani and Basol in its March 19, 2018 Invalidity Contentions, which predate the '922 and '672 Petitions (*see* ECF No. 588-13 ("Invalidity Contentions") at 38, 62). VLSI presents evidence that Intel disclosed Willingham and Khellah in the '922 Petition. *See* Petition for Inter Partes Review of U.S. Patent No. 8,004,922 at 1, 3, 10 *Intel Corp. v. VLSI Tech. LLC*, No. IPR2018-01033 (P.T.A.B. June 21, 2018). And VLSI presents evidence that Intel disclosed Shibata and Pahl in its '672 Petition. Petition for Inter Partes Review of U.S. Patent No. 8,268,672 at 1, *Intel Corp. v. VLSI Tech. LLC*, No. IPR2018-01107 (P.T.A.B. June 13, 2018). Thus, VLSI argues, the Court should grant summary judgment of no invalidity as to combinations (2), (3), and (6) because "[t]hese combinations consist entirely of references Intel explicitly disclosed as prior art at the time it filed its IPR petitions, and are thus estopped under Section 315(e)(2)." VLSI Mot. at 18.

In response, Intel concedes that "the Federal Circuit has held that IPR estoppel attaches to 'all grounds . . . which reasonably could have been asserted against the claims included in the petition.'" Intel Opp. at 24–25 (quoting *Broadcom*, 25 F.4th at 991). Intel states that it seeks to preserve its position that IPR estoppel should not bar these prior art grounds because the plain text of the estoppel statute provides that IPR estoppel applies to "any ground that the petitioner raised

or reasonably could have raised during that inter partes review," 35 U.S.C. § 315(e)(2).

The Federal Circuit recently held in *Broadcom* that, where it is "undisputed" that a patent challenger was "aware of the prior art references that [it] sought to raise in the district court when [it] filed its IPR petitions," "summary judgment . . . of no invalidity based on IPR estoppel" is warranted. 25 F.4th at 991, 995. Although Intel wishes to preserve its argument that *Broadcom* was wrongly decided, it acknowledges that this Court must follow *Broadcom*. As such, VLSI's Motion for Summary Judgment that IPR estoppel precludes Intel from relying on the three obviousness combinations – (2) Rakshani and Willingham; (3) Rakshani and Khellah; and (6) Pahl, Shibata, and Basol – is granted.

b. Okada, Zakel, and the Lee Book

Second, VLSI seeks summary judgment that IPR Estoppel bars Intel from obviousness combination (4) Okada, Zakel, and the Lee Book because "Intel was aware of or reasonably could have raised the Lee Book at the time it filed the '672 Petition." VLSI Mot. at 19–20.

Intel responds that it does not rely on a combination of Okada, Zakel, and the Lee Book, but instead Intel says that it has asserted "applicant admitted prior art ('AAPA')—i.e., admissions regarding prior art contained in the '672 Patent—in combination with the Lee Book." Intel Opp. at 23–24 (citing Fay Report ¶¶ 139–88). Intel notes that "VLSI does not move for summary judgment based on that combination, and instead argues that 'VLSI is entitled to summary judgment of no invalidity concerning Intel's combination of Okada, Zakel, and Lee Book.'" Mot. 20.

The Court agrees with Intel. VLSI's motion clearly addresses only the combination of Okada, Zakel, and the Lee Book. The parties' discussion in the Intel Opp. at 23 and VLSI Reply at 9 about whether Intel's assertion of the combination of AAPA and the Lee Book is barred under IPR estoppel is not properly before the Court and will not be considered. VLSI's Motion for Summary Judgment that IPR estoppel precludes Intel from relying on (4) Okada, Zakel, and the Lee Book is granted; but the motion is denied with respect to a combination of AAPA and the Lee Book (Fay Report ¶¶ 139–88).

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c. The Nehalem Processor And P1264 Process

Third, VLSI seeks summary judgment that IPR Estoppel bars Intel from using two obviousness combinations for its purportedly improper reliance on physical products – (1) Nehalem, Gunther, and Willingham (relied on by Dr. Apsel); and (5) Okada, the Lee Book, and the Intel P1264 Package Process (relied on by Dr. Fay).

While physical products cannot be raised during IPR proceedings, IPR estoppel can apply to patents and printed publications, including those "that relate to and describe a physical product." *Wasica Fin. GMbH v. Schrader Int'l, Inc.*, 432 F. Supp. 3d 448, 453 (D. Del. 2020). That said, several courts have found that "reliance on some printed publications in an overall collection of documents being used to describe a system invalidity theory should not lead to estoppel of the overall system invalidity theory itself, nor piecemeal exclusion of the printed publications underlying that system invalidity theory[.]" *SPEX Techs. Inc. v. Kingston Tech. Corp.*, 2020 WL 4342254, at *15 (C.D. Cal. June 16, 2020); *CliniComp Int'l, Inc. v. Athenahealth, Inc.*, 2020 WL 7011768, at *2 (W.D. Tex. Oct. 28, 2020) (finding no IPR estoppel when the expert "does not rely solely on publicly available documents" but "opinions [we]re [also] supported by non-public documents and other information that are not 'printed publications'" that could have been raised in IPR proceeding).

Several district courts have addressed whether printed materials that describe physical products can be allowed. For example, one court found that a physical device cannot be used to argue invalidity if the "material limitations" are disclosed in patents and printed publications; another held the same if the physical device is "adequately described in" the printed publications. *Bos. Sci. Corp. v. Cook Grp. Inc.*, 2023 WL 1452172, at *34 (S.D. Ind. Jan. 31, 2023) (a defendant cannot "us[e] a physical device to argue invalidity if all of the material limitations of that device were disclosed in a patent or printed publication that the patent challenger either knew about or reasonably could have discovered."); *Avanos Med. Sales, LLC v. Medtronic Sofamor Danek USA, Inc.*, 2021 WL 8693677, at *2 (W.D. Tenn. Oct. 8, 2021) (where a defendant claims to rely on "product" or "system" prior art, estoppel still applies when "the relevant claim limitations . . . [are] adequately described in [] publicly available documents.").

Furthermore, several courts have held that physical inspection is not always necessary, particularly when a plaintiff "does not contend that the documentation fails to describe the product accurately." *SiOnyx, LLC v. Hamamatsu Photonics K.K.*, 330 F. Supp. 3d 574, 604 (D. Mass. 2018); *see also IOENGINE, LLC v. PayPal Holdings, Inc.*, 607 F. Supp. 3d 464, 512 (D. Del. 2022) (holding that the "expert need not have inspected or tested the devices in order to rely upon them for purposes of invalidity" because "[c]ourts . . . have allowed the functions of prior art devices to be established through the use of documents and testimony" (citing *SiOnyx*, 330 F. Supp. 3d at 604). However, one court cautioned, "[i]f a defendant 'purport[s] to rely on a device without actually relying on the device itself' . . . , the policy behind IPR estoppel may best be served by excluding that reference." *In re Koninklijke Philips Pat. Litig.*, 2020 WL 7392868, at *27 n.25 (N.D. Cal. Apr. 13, 2020).

i. Nehalem Processor

VLSI seeks to bar Intel from using combination (1) Nehalem, Gunther, and Willingham. VLSI argues that Dr. Apsel facially relies on the Nehalem Processor, but did not actually examine a physical Nehalem product for her analysis and instead relied on Intel documents describing the product. ECF No. 588-16 (Apsel Report Ex. B) at 1–26 (not listing any physical products as "Materials Considered"). VLSI also argues that Dr. Apsel relies on the "Nehalem HC" and "Nehalem IDF" slide decks for every element she opines that the Nehalem processor discloses in her obviousness analysis. VLSI Mot. at 22; *see, e.g.*, Apsel Report ¶ 777 ("Nehalem is a system-on chip . . . as shown below [in Nehalem IDF]."), ¶ 793 ("As shown below [in Nehalem HC], each Core, including Core 1 . . . is supplied by a voltage . . . through a power gating transistor[.]"). VLSI further argues that the Nehalem HC and Nehalem IDF slide decks are publicly available prior art publications that Intel disclosed in its March 19, 2018 Invalidity Contentions. VLSI Mot. at 22 (citing Invalidity Contentions at 38–39). VLSI does acknowledge that Dr. Apsel's Nehalem obviousness analysis also includes citations to an "Intel Tech Journal" document dated in 2010, after the undisputed 2009 priority date for the '922 Patent, but argues that "The 'Intel Tech Journal' document is not prior art, and Dr. Apsel relies on it exclusively to bolster her discussion of Nehalem HC and Nehalem IDF." *Id.* at 23 (citing Apsel Report ¶ 780).

In response, Intel argues that Dr. Apsel does not rely entirely on published materials, but rather the Nehalem Processor as described in the Intel Tech Journal. Intel identifies vast citations by Dr. Apsel to the Intel Tech Journal and argues that it discloses details regarding how the prior-art Nehalem product worked before the '922 Patent was filed. Intel Opp. at 18 (citing Apsel Report at ¶¶ 780–83, 804, 807, 820–21, 827, 833, 836, 839–40, 844, 847, 851–52, 854–55, 860, 862, 870, 872, 890, 894, 902, 915, 921, 923, 930, 935–37, 940, 943, 946, 949, 953, 956–57, 959–60). Intel then shows Dr. Apsel's specific reliance "on infrared emission physical device images of Nehalem from the Intel Tech Journal [and not found anywhere in the Nehalem HC or Nehalem IDF presentations] as evidence that the Nehalem cores '[we]re controlled separately from the rest of the SoC (the 'uncore') by powering [on or] off while the uncore remains powered." *Id.* (quoting Apsel Report ¶¶ 782–83, ECF No. 672-7 ("Intel Tech Journal") at 56, 58–59). Intel argues that Dr. Apsel also relies on an internal Intel Nehalem Microarchitectural Specification ("MAS") document that could not be used in an IPR proceeding because it is not a "printed publication." *Id.* The document purportedly "[redacted]" *Id.* at 19–20 (citing Apsel Report ¶ 824).

In reply, VLSI argues that none of the additional evidence describing the Nehalem Processor is necessary for Dr. Apsel's obviousness opinion. VLSI Reply at 12–13. VLSI attacks paragraphs 780–83 of the Apsel Report for echoing the Nehalem HC and IDF presentations. As for the MAS document, VLSI argues that Dr. Apsel uses the MAS solely to demonstrate the background knowledge of a person of ordinary skill, and not as prior art. VLSI also argues that "the fact that Dr. Apsel did not actually examine the Nehalem processor itself is strong evidence that Intel and Dr. Apsel are using the Nehalem processor solely to circumvent IPR estoppel." VLSI Reply at 12; *see Philips*, 2020 WL 7392868, at *27 n.25, *Medline Indus., Inc. v. C.R. Bard, Inc.*, 2020 WL 5512132, at *5 (N.D. Ill. Sept. 14, 2020) ("[T]he petitioner cannot put forth invalidity arguments in litigation that rely solely upon patents or printed publications that could have been raised in the IPR, and then claim that IPR estoppel does not apply because these printed materials reflect or represent a prior art product.").

The Court agrees with Intel regarding Dr. Apsel's reliance on the Intel Tech Journal.

Although VLSI lays out an argument for why four paragraphs (¶¶ 780–83) are duplicative of Nehalem HC and Nehalem IDF, VLSI does not sufficiently address the remainder of Intel's citation to the Apsel Report. Apsel Report at ¶¶ 804, 807, 820–21, 827, 833, 836, 839–40, 844, 847, 851–52, 854–55, 860, 862, 870, 872, 890, 894, 902, 915, 921, 923, 930, 935–37, 940, 943, 946, 949, 953, 956–57, 959–60 (describing the product). The Court cannot parse and compare each of these citations to Nehalem HC and Nehalem IDF without more from VLSI that shows that the "material limitations of that device were disclosed" (*Bos. Sci. Corp.*, 2023 WL 1452172, at *34 or that the "relevant claim limitations . . . [are] adequately described" (*Avanos*, 2021 WL 8693677, at *2) in the two presentations. Furthermore, the Intel Tech Journal is not prior art because it is dated in 2010, after the'922 Patent was filed on June 5, 2009. Intel Opp. at 18; '922 Patent. Since the Intel Tech Journal is clearly not prior art and Intel could not have relied on it at IPR, the motion is denied on this basis. *SPEX*, 2020 WL 4342254, at *15; *CliniComp*, 2020 WL 7011768 at *2. Furthermore, since the Intel Tech Journal could not be used in IPR, VLSI's argument that Dr. Apsel's failure to inspect the Nehalem Processor suggests an attempt to circumvent IPR estoppel is also not persuasive. *Philips*, 2020 WL 7392868, at *27 n.25; *Medline*, 2020 WL 5512132, at *5.

Thus, the Court concludes that a genuine dispute of material fact remains with respect to whether combination (1) relies entirely on published prior art or also the Nehalem Processor as described in the Intel Tech Journal. VLSI's Motion for Summary Judgment that IPR estoppel precludes Intel from relying on (1) Nehalem, Gunther, and Willingham is denied.

ii. P1264 Process

VLSI seeks to bar Intel from using combination (5) Okada, Lee Book, and Intel P1264 Package Process. VLSI similarly argues that Dr. Fay did not examine anything relating to the P1264 Process for his analysis. ECF No. 588-17 (Fay Report App'x B) at 1–5 (not listing any physical products as "Materials Considered"). VLSI also argues that Dr. Fay does not rely on the P1264 Process to disclose any claim element that is not also disclosed by the Lee Book or Okada, making the P1264 Process cumulative. Alternatively, VLSI argues that even if Dr. Fay's use of the P1264 Process was not duplicative of Okada and the Lee Book, the elements Dr. Fay draws on

the P1264 Process for were disclosed in prior art printed publications written by Intel engineers ("Yeoh"), meaning Intel reasonably could have raised these same arguments during IPR.

Intel responds that inspection is not a predicate to use and that "it would be particularly unfair to do so in circumstances like here where Dr. Fay is relying on a prior art process used two decades ago and no longer in use today." Intel Opp. at 22. Intel further argues that it "can assert invalidity based on grounds that might be 'cumulative or redundant' of grounds raised during IPR as long as it does so by relying on references or combinations of references that were unavailable." *Id.* (quoting *Contour IP Holding, LLC v. GoPro, Inc.*, 2020 WL 109063, at *6 (N.D. Cal. Jan. 9, 2020)); see also *Pact XPP Schweiz AG v. Intel Corp.*, 2023 WL 2631503, at *6 (D. Del. Mar. 24, 2023) ("PACT tries to string together printed references that it claims are 'cumulative' of the physical products. But PACT hasn't pointed me to any legal basis to parse Intel's legal contentions to decide whether the physical device portion is 'cumulative.'"). Intel also disputes that the P1264 Process is cumulative because "Okada did not teach [redacted] used in the P1264 Package Process." *Id.* at 23 (quoting ECF No. 671-5 ("Fay Reply") ¶ 38). Intel also argues that "Yeoh was published in 2006—i.e., after VLSI's claimed priority date of May 6, 2004 and the April 28, 2005 U.S. filing date of the '672 Patent" and therefore "Yeoh is not prior art, and thus could not have been asserted as a prior art reference in the IPR." *Id.*

In reply, VLSI distinguishes *Contour IP*, arguing that "it was decided before the Federal Circuit's decision in *Broadcom*, and thus relied on now-outdated reasoning in determining that estoppel did not prevent the defendant from raising prior art references cumulative of grounds raised in the IPR." VLSI Reply at 15. VLSI adds that "Dr. Fay ***never relies on*** [redacted] allegedly used in the P1264 Process for his invalidity arguments." *Id.* (emphasis in original).

The Court agrees with Intel. Intel has shown that there are genuine factual disputes as to whether Yeoh was available during IPR and whether Dr. Fay relied on the copper pillar in his obviousness analysis. The Court need not settle the parties' dispute over *Contour IP* because there is a factual dispute over whether the physical prior art is cumulative. *See Pact XPP*, 2023 WL 2631503 at *6 ("Intel disputes whether the documents PACT cites were either available to it or include all the relevant features of the physical product, and its expert will testify that the

combination of the physical and printed prior art is significant. I have no basis to disregard such testimony and those references."). On this basis, VLSI's Motion for Summary Judgment that IPR estoppel precludes Intel from relying on (5) Okada, the Lee Book, and the Intel P1264 Package Process is denied.

B. Intel's Motion

Intel separately moves for summary judgment on the following grounds: (1) no infringement of the '836 Patent, (2) no infringement of the '922 Patent, (3) invalidity of the asserted claims for the '922 Patent, (4) no infringement of the '806 Patent, (5) no infringement of the '672 Patent, (6) that it is licensed to use the Asserted Patents, and (7) no willful infringement, no indirect infringement, and no enhanced damages for any patent.

1. Infringement of the '836 Patent

VLSI accuses Intel's Turbo Boost Max Technology 3.0 ("TBMT") and "Thread Director" of infringing claims 1, 9–11, 13, 17, 20, and 21 of the '836 Patent. Intel Mot. at 1–2. Each of Intel's Accused Products includes multiple cores and a storage device that stores a processing speed parameter (e.g., maximum measured frequency) for each core. ECF No. 579-4 ("Conte Report") ¶¶ 307–407. Each Accused Product also includes a power control unit ("PCU") functioning as the brains of the power management architecture, and includes hardware circuitry and a microcontroller that runs special firmware code called Pcode (or p-code). *Id*. ¶ 278.

Claim 1 reads in relevant part:

> A method for operating a multi-core processing device, comprising:
> . . .
> ***upon identifying*** a processing task that can not be run across the plurality of cores, ***selecting*** a core from the plurality of cores having a fastest measured processing speed parameter at a given voltage to run the processing task.

'836 Patent at 10:44–54 (emphasis added). Claim 20 reads in relevant part:

> In a multi-core processor comprising multiple cores . . . a method for executing single core applications and multi-core applications comprising: . . .
>
> running a single core application on a single core ***which is identified*** from the stored maximum processing speed values for the multiple cores as being the fastest core ***upon identifying*** a processing task that

> cannot be run across the plurality of the multiple cores.

Id. at 12:17–30 (emphasis added). Claim 10 contains similar language:

> A multi-core system on chip (SOC), comprising: . . .
>
> at least a first storage device for storing the performance parameter values for the plurality of cores for use in ***selecting*** a core having maximized or minimized performance parameter value at a specified voltage to run a processing task that can not be run across the plurality of cores.

Id. at 11:19–29 (emphasis added). In its Markman Order, the Court construed claim 10 to include the same "upon identifying" limitation as claims 1 and 20. Markman Order at 22–25. Claim 9 depends on claim 1; claims 11, 13, and 17 depend on claim 10; and claim 21 depends on claim 20.

Intel makes three arguments that TBMT and Thread Director do not infringe the '836 Patent: (1) there is no literal infringement (*id.* at 3–4); (2) there is no infringement under the doctrine of equivalents ("DOE") (*id.* at 4–6); and (3) there is no infringement because testing occurs outside the United States (*id.* at 6–8). The Court addresses the three arguments in turn.

a. Literal Infringement

Intel first argues that the plain language of the "upon identifying" limitation (claims 1, 9–11, 13, 17) and "identifying" limitation (claims 20, 21) specify that selecting the core to run a single-core task occurs only ***after*** identification of the task as a single-core task. Intel Mot. at 3–4. Intel cites evidence that VLSI argued that the claims contain a temporal requirement that the task is identified as single-core before a core is selected. ECF No. 143 (VLSI Markman Brief) at 20 (agreeing "upon identifying" is "a temporal term that describes ***when*** something happens") (emphasis added); ECF No. 145 (Conte Markman Decl.) ¶ 181 (same); ECF No. 158-13 ("'836 File History") at 1934 (Examiner requiring applicants "to amend independent claims 1, 10, and 20 to clarify that a core is selected from the plurality of cores ***when*** it is identified that a task cannot be run across the plurality of cores" as a condition for allowing the patent to issue) (emphasis added). Intel also cites to depositions of several fact witnesses as evidence that "the accused products never identify whether a task is a single-core task—let alone before selecting a core for the task." Intel Mot. at 3 (citing ECF No. 580-5 (Ramani Dep.), ECF No. 579-6 (McGavock Dep.), ECF No. 580-8 (Therien 1/27/23 Dep.), ECF No. 580-9 (Chen Dep.), ECF No. 579-7 (L.

Brown Dep.), ECF No. 579-8 (Fenger Dep.), ECF No. 579-9 (T. Brown Dep.)). Intel then attacks VLSI expert Dr. Thomas M. Conte's opinion, writing that Dr. Conte points only to an identification process that "occurs after a core has already been selected or identified." Intel Mot. at 4 (citing Conte Report ¶¶ 416–17, 427, 433, 439, 448, 454, 460, 466), ECF No. 579-5 (Conte Dep.) 136:23–139:23, 138:2–15),

VLSI responds that Intel mischaracterizes Dr. Conte's infringement opinion. VLSI Opp. at 3. VLSI argues that "Dr. Conte does not contend that the OS-based scheduler software alone performs the 'selecting' step" but instead "the step is performed by the combination of the OS software working together with the PCU's Pcode." *Id.* (citing Conte Report ¶ 417). VLSI also points to Dr. Conte's deposition, where he "repeatedly refuted the central premise of Intel's motion, that 'what Dr. Conte points to in the accused products as identifying a single-core task (i.e., the code determining how many cores are active) occurs after a core has already been selected or identified.'" *Id.* (citing ECF No. 579-5 (Conte Dep.) 135:12–136:2, 134:17–135:11, 136:12–140:6). VLSI also dismisses the fact witness testimony, stating that it "only focused on the OS scheduler in isolation and not the operation of the system as a whole, including the involvement of the Pcode in the 'selecting' step" and that "many of these witnesses testified that they were not familiar with or had not seen the Accused Products' Pcode." VLSI Opp. at 4.

Intel replies that it's not about "which components are involved in the accused identifying/selecting steps, including the role of p-code" but rather, "the order that the accused identifying/selecting steps occur, not which components or p-code are involved in those steps." Reply at 1. To that, Intel argues, "the undisputed evidence shows that Intel's accused products do not select a core after identifying a single-core task as required by the 'upon identifying' limitation." *Id.*

The Court agrees with VLSI. Dr. Conte's report opines that the p-code works in conjunction with the OS to pick a single favored core to run a single active thread:

> In . . . TBMT and Thread Director, Pcode working in conjunction with Intel-authored software (for OS versions 7, 8, and 10 TH1), and/or the OS, performs the step of "selecting a core . . . to run the processing task." Pcode in an accused processor provides core diversity information (e.g., measured max frequency of each core) to the Intel-

> authored software and/or OS, which in turn ***causes a single-active thread to be scheduled on a "favored" core*** (e.g., a core having a fastest frequency) based on the core diversity information received from the Pcode.

Conte Report at ¶ 417 (emphasis added). Dr. Conte's report then states that the selecting step is performed "upon identifying the single core task." *Id.* He continues:

> Further, the "selecting" claim step is performed "upon identifying a single core task." Pcode working in conjunction with Intel-authored software and/or the OS ***identifies a single-core task***. In particular, the Intel-authored software and/or OS schedules a thread on the favored core (e.g., as explained herein), and the remaining cores enter sleep states. The Pcode detects that the favored core is the only active core (e.g., the only core in C0 state***), and causes the favored core to run the scheduled single-core task*** at the fastest measured operating frequency at a given voltage.

Id. (emphasis added). Contrary to Intel's argument (Mot. at 4), the Court finds that Dr. Conte's report is evidence that the accused technology identifies a task, then selects a core to run that task.

Dr. Conte's deposition testimony does not fatally undermine the conclusion in his report. For example, when Dr. Conte is asked about core selection for a single-core task, Dr. Conte states that "the p-code presents diversity information to the operating system which allows that operating system to select the favored core." ECF No. 579-5 (Conte Dep.) 139:12–15. The Court finds that Dr. Conte's report and deposition testimony create a genuine dispute of material fact as to whether TBMT and Thread Director meet the "upon identifying" claim limitation. Thus, Intel's Motion for Summary Judgment of no literal infringement of the '836 Patent for failure to meet the temporal limitation is denied.

b. Doctrine of Equivalents

VLSI presents a theory under the doctrine of equivalents (DOE) where the "selecting" step can occur "upon *or substantially simultaneously with* identifying a single core task" (instead of upon identifying a single core task). VLSI Opp. at 7 (quoting Conte Report ¶¶ 471–72). Intel makes three arguments that VLSI's DOE theory fails as a matter of law: amendment-based estoppel, argument-based estoppel, and claim vitiation. Intel Mot. at 4–6. The Court addresses each in turn.

i. Amendment-Based Estoppel

First, Intel argues that "amendment-based prosecution history estoppel forecloses VLSI

from alleging any broader scope for this claim limitation under the DOE." *Id.* at 4–5. Intel explains that "[d]uring prosecution, claim 20 was narrowed by amendment to add the limitation 'upon identifying a processing task that cannot be run across the plurality of the multiple cores.'" *Id.* at 4 (quoting '836 File History at 1941). Intel continues that "[t]he applicants relied on [the multiple cores] claim language during prosecution to distinguish the prior art that disclosed selecting cores for other reasons." *Id.* at 4–5 (citing '836 File History).

VLSI argues that the Applicant's agreement to amend claim 20 does not trigger prosecution history estoppel because the clarifying amendment was not made to overcome the prior art. VLSI Opp. at 5. VLSI continues that "the addition of 'upon identifying' to claim 20 'did nothing more than make express what had been implicit in the claim as originally worded,' as this language had been present in claims 1 and 10 from the beginning." *Id.* (quoting *Interactive Pictures Corp. v. Infinite Pictures, Inc.*, 274 F.3d 1371, 1377 (Fed. Cir. 2001)).

VLSI argues alternatively that "amendment to claim 20 does not trigger prosecution history estoppel because the order or timing of events (upon identifying before selecting) had nothing to do with the Examiner's initial rejection of the claims." VLSI Opp. at 6. Rather, "[t]he issue was whether the prior art disclosed the 'identifying' limitation at all." *Id.* (citing '836 File History at 1877–79, 1904–06, 1913–1916).

Intel replies that the "amendment (1) added an entirely new temporal limitation to claim 20, and (2) arose from an Examiner interview discussing the obviousness of the claim (over the prior art Bernstein reference), after which the Examiner expressly conditioned allowance of the claim on making the amendment." Intel Reply at 2.

The Court agrees with VLSI. As VLSI notes, claims 1 and 10 were not narrowed during prosecution. VLSI Opp. at 5 (citing '836 File History at 1824–25). The only independent claim where this language was added is claim 20. Furthermore, VLSI presents evidence that the examiner withdrew the rejection of all claims and suggested that "upon identifying" is clarifying language. *Id.* (citing '836 File History at 1928, 1934, 1936, 1938–41). Thus, the Court finds that this evidence creates a genuine issue of material fact that forecloses a finding of amendment-based estoppel at summary judgment.

ii. Argument-Based Estoppel

Second, Intel argues that "argument-based prosecution history estoppel also bars VLSI's equivalents theory" because of VLSI's "repeated reliance on the 'upon identifying' limitation to distinguish every asserted claim from the prior art during prosecution." Intel Mot. at 5 (citing '836 File History). Intel's motion points to several parts of the '836 File History where the applicant claimed a temporal aspect. Intel Mot. at 5; *see, e.g.*, '836 File History at 1877 (applicant stating "claims 1, 10, and 20" all require "upon identifying a single-core processing task that cannot be run by the plurality of cores, the core having the fastest measured processing speed parameter is selected to run the identified single-core processing task"); *id.* at 1913–14 (same); *id.* at 1934 ("It was agreed to amend independent claims 1, 10, and 20 to clarify that a core is selected from the plurality of cores when it is identified that a task cannot be run across the plurality of cores.").

VLSI responds that its "DOE theory does not eliminate the identification of a single core task, but rather concerns its timing with respect to the 'selecting' step" and specifically, "that 'selecting' can occur 'upon or substantially simultaneously with identifying a single core task.'" VLSI Opp. at 7 (quoting Conte Report ¶¶ 471–72). VLSI specifically refutes the citation to page 1934 of the prosecution history, stating that it is not enough that "the Examiner used the term 'when' in interview summary" because "the interview focused on changing the word 'by' to 'across,' and the word 'when' was not added to the claims." VLSI Opp. at 7; '836 File History at 1934, 1936, 1938–41.

In its reply, Intel adds a fourth citation to the file history. Intel Reply at 3 (quoting '836 File History at 1876) ("[A] 'single core' processing task is identified. Once a 'single core' task is identified (a.k.a., a processing task that cannot be run by the plurality of cores), the claimed methodology selects the fastest core to run the 'single core' task.").

The Court agrees with VLSI. "To invoke argument-based estoppel, 'the prosecution history must evince a clear and unmistakable surrender of subject matter." *Amgen, Inc. v. Coherus BioSciences, Inc.*, 931 F.3d 1154, 1159 (Fed. Cir. 2019) (quoting *Conoco, Inc. v. Energy & Envtl. Int'l, L.C.*, 460 F.3d 1349, 1364 (Fed. Cir. 2006)). "Clear assertions made during prosecution in

support of patentability, whether or not actually required to secure allowance of the claim, may also create an estoppel . . . the relevant inquiry is whether a competitor would reasonably believe that the applicant had surrendered the relevant subject matter." *Id.* at 1159–60 (quoting *PODS, Inc. v. Porta Stor, Inc.*, 484 F.3d 1359, 1368 (Fed. Cir. 2007)) (cleaned up).

The four statements put forth by Intel are not enough to prevail at summary judgment. The first two merely recite claim language. '836 File History at 1877 (applicant stating "claims 1, 10, and 20" all require "upon identifying a single-core processing task . . ."); *id.* at 1913–14 (same). A finding that a recitation of claim language alone would estop an equivalent theory of infringement would undo the doctrine of equivalents. The third citation, that "a core is selected from the plurality of cores when it is identified that a task cannot be run across the plurality of cores" is also not enough. As VLSI argues, the word "when" was provided by the examiner, not the applicant. Finally, the Court does not consider the fourth citation ('836 File History at 1876) because Intel did not raise it until its reply brief, and has therefore waived the argument. Thus, the Court finds that this evidence creates a genuine issue of material fact that forecloses a finding of argument-based estoppel at summary judgment.

iii. Claim Vitiation

Intel's final argument is that VLSI's DOE theory would vitiate the Asserted Claims of the '836 Patent. The doctrine of claim vitiation "ensures that 'the application of the doctrine of equivalents is not allowed such broad play as to effectively eliminate a claim element in its entirety.'" *Bio-Rad Lab'ys, Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1366 (Fed. Cir. 2020) (quoting *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29 (1997)) (cleaned up). Vitiation "is not an exception or threshold determination that forecloses resort to the doctrine of equivalents, but is instead a legal conclusion of a lack of equivalence based on the evidence presented and the theory of equivalence asserted." *Id.* at 1366–67 (quoting *UCB, Inc. v. Watson Labs., Inc.*, 927 F.3d 1272, 1283 (Fed. Cir. 2019)). "[S]aying that a claim element would be vitiated is akin to saying that there is no equivalent to the claim element in the accused device based on the well-established 'function-way-result' or 'insubstantial differences' tests." *Id.* at 1366–67 (quoting *Brilliant Instruments, Inc. v. GuideTech, LLC*, 707 F.3d 1342, 1347 (Fed. Cir.

2013)).

"The vitiation test cannot be satisfied merely by noting that the equivalent substitute is outside the claimed limitation's literal scope." *Brilliant*, 707 F.3d at 1347. Rather, "vitiation comes into play when the alleged equivalent is 'diametrically opposed to the missing claim element." *Bio-Rad*, 967 F.3d at 1367 (internal quotations omitted). One way to show a claim is vitiated is "if the theory or evidence of equivalence is legally incapable of establishing that the differences between the limitation in the claim and the accused device are insubstantial; i.e., if the theory or evidence is so legally insufficient as to warrant a holding of non-infringement as a matter of law." *Id.* (quoting *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1017 (Fed. Cir. 2006)). "If the claimed and accused elements are recognized by those of skill in the art to be opposing ways of doing something, they are likely not insubstantially different." *Id.* (quoting *Brilliant*, 707 F.3d at 1347–48).

Intel argues that VLSI's DOE theory "would vitiate the 'upon identifying' limitation by allowing the claims to be met if a single-core task is sent to the fastest core for any reason, including those having nothing to do with whether the task is a single-core task." Intel Mot. at 6.

VLSI responds that under its DOE theory, "the claims are met if a single-core task is identified substantially simultaneously with selecting the fastest core to run the single-core task" because "when a single-core task is identified and placed on the fastest (favored) core, the core's clock frequency is boosted to its maximum measured frequency, which is higher than the maximum measured frequency of the non-favored cores." VLSI Opp. at 7 (citing Conte Report ¶¶ 417, 471–472).

The Court agrees with Intel that VLSI's DOE theory where a single-core task can be identified "substantially simultaneously" would vitiate the claims. The literal meaning of the claim limitations requires the two-step process of first identifying the task and then selecting the core. VLSI's "substantially simultaneously" theory allows for any "ordering of the identification and selection steps—such that the identification step could occur before, after, or simultaneously with the selection step." *See* Intel Reply at 3. That is not merely interchangeable or outside the claimed limitation's literal scope, but would "effectively eliminate" the upon identifying "claim

element in its entirety." *Bio-Rad*, 967 F.3d at 1366. VLSI's explanation that a core's frequency can be boosted does not save its theory. That a core can be sped up has nothing to do with the order in which the steps in a process are accomplished, and thus says nothing about whether the equivalent process is "substantially similar" to the literal process.

Having found as a matter of law that it would vitiate the Asserted Claims of the '836 Patent, the Court finds that VLSI's DOE theory fails as a matter of law. Intel's Motion for Summary Judgment of no infringement of the '836 Patent under the doctrine of equivalents is granted.

c. Testing Outside the Country

Intel argues that the Court should find no infringement of the '836 Patent because certain limitations were infringed only outside the United States. Among the Asserted Claims are four method claims (claims 1, 9, 20, and 21) and four apparatus claims (claims 10–11, 13, and 17). The Court addresses the method claims, then the apparatus claims.

i. Method Claims

"A defendant can only directly infringe a method claim . . . by 'using' the method within the United States, which requires that the defendant practice every step of the method within the United States." *France Telecom S.A. v. Marvell Semiconductor Inc.*, 82 F. Supp. 3d 987, 993 (N.D. Cal. 2015) (citing *Meyer Intellectual Properties Ltd. v. Bodum, Inc.*, 690 F.3d 1354, 1366 (Fed. Cir. 2012)); *NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1318 (Fed. Cir. 2005) ("[A] process cannot be used 'within' the United States as required by section 271(a) unless each of the steps is performed within this country."), *abrogated on other grounds*, *see IRIS Corp. v. Japan Airlines Corp.*, 769 F.3d 1359, 1361 n.1 (Fed. Cir. 2014).

Claims 1, 9, 20, and 21 recite methods that, among other things, require "measuring" the processing speed of each core in a multicore processor. According to Intel, "VLSI alleges that Intel performs the claimed 'measuring' step only when Intel tests its products during manufacturing." Intel Mot. at 6 (citing Conte Report ¶¶ 307–63, 541–45, ECF No. 579-5 (Conte Dep.) 84:8–85:23). Intel, however, argues that "it is undisputed that Intel performs this testing exclusively in Costa Rica and Malaysia. *Id.* (citing ECF No. 580-7 (Therien 1/26/23 Dep.)

181:17–25, ECF No. 580-8 (Therien 1/27/23 Dep.) 399:20–400:9, ECF No. 580-13 ("Cavagnaro Dep.") 158:16–159:19, 160:19–161:6, Johnson Dep. 41:23–25).

VLSI responds in two parts. First, VLSI points to a 33-page excerpt of the Conte Report as evidence that "Intel meets the technical requirements of the 'measuring' limitation." VLSI Opp. at 8 (citing Conte Report ¶¶ 307–63). Second, VLSI argues that Intel stipulated that 70% of the activities that meet the technical requirements are deemed to have a U.S. nexus under 35 U.S.C. 271(a). The stipulation states:

> Of the total, global number of Intel products and associated activities determined (without regard to geographic considerations) to meet the technical requirements of any asserted VLSI patent claim not proven invalid by Intel[,] . . . seventy percent (70%) thereof will be deemed to have a United States nexus as required by each subsection of 35 U.S.C. § 271 and for determining any patent infringement damages in this case. . . .

ECF No. 581-2 ("U.S. Nexus Stip.") at 2. VLSI argues that "[t]he stipulation forecloses Intel from arguing that it does not infringe solely due to geographical considerations, which is what Intel is arguing here." VLSI Opp. at 8.

The Court agrees with Intel. As an initial matter, VLSI has not pointed the Court to any evidence from Dr. Conte's Report that the testing occurs in the United States. In the only part of the lengthy excerpt provided to the Court that addresses the location of testing, Dr. Conte does not dispute that testing occurs outside the United States. Conte Report at ¶ 322 ("HVM testing is developed in Oregon and sent out to the Intel manufacturing facilities across the world."). Dr. Conte's report does not supply evidence of testing occurring inside the United States, and in fact is an acknowledgement that testing occurs outside the United States.

Instead, VLSI relies entirely on the stipulation for its argument that the testing is deemed to have occurred inside of the United States. But the stipulation expressly states that it is not an admission of infringement. U.S. Nexus Stip. at 2 ("By entering into this agreement, neither party makes any admission about patent infringement . . . ."); *id.* ("This agreement does not in any way suggest or indicate that any of the Intel products at issue infringe . . . ."). Furthermore, the stipulation states that the nexus only applies to products determined to meet the technical requirements of any asserted claim, such as infringement. *Id.* ("Of the total, global number of

Intel products and associated activities determined (without regard to geographic considerations) to meet the technical requirements of any asserted VLSI patent claim . . . will be deemed to have a United States nexus."). One of the technical requirements necessary for the nexus to apply is that the claim limitations are met (in the United States). Since the testing limitation is a condition of finding nexus under the stipulation, the stipulation cannot be used as evidence of meeting the testing limitation. Thus, the Court concludes that the stipulation is not evidence that Intel meets the testing limitation.

Having found that VLSI's evidence does not create a genuine dispute of material fact as to whether the testing limitation occurs in the United States, the Court finds as a matter of law that VLSI cannot prove that Intel infringes claims 1, 9, 20, and 21 of the '836 Patent. Thus, Intel's Motion for Summary Judgment of no infringement of claims 1, 9, 20, and 21 of the '836 Patent is granted.

ii. Apparatus Claims

"[W]here claim language recites 'capability, as opposed to actual operation,' an apparatus that is 'reasonably capable' of performing the claimed functions 'without significant alterations' can infringe those claims." *INVT SPE LLC v. Int'l Trade Comm'n*, 46 F.4th 1361, 1375–76 (Fed. Cir. 2022) (quoting *ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1362 (Fed. Cir. 2018)).

Claims 10, 11, 13, and 17 recite a "system on a chip" that, among other things, contains "a performance measurement circuit ***for measuring a performance parameter value*** for said core." '836 Patent at 11:20–23 (emphasis added). VLSI alleges that "the accused products contain circuitry that satisfies this 'measuring' limitation." *See* Intel Mot. at 7 (citing Conte Report ¶ 493). However, Intel argues "it is undisputed that the accused circuitry is only used for measuring values when connected to an external testing device called an 'ATE tester' that is part of Intel's manufacturing facilities in Costa Rica and Malaysia." *Id.* (citing Cavagnaro Dep. 158:16–159:19, 160:19–161:6, 166:16–167:8, 170:2–171:18, ECF No. 579-5 (Conte Dep.) 109:21–110:6, Conte Report ¶ 339).

VLSI responds that "[t]he ATE tester is not a required component of the claimed 'performance measurement circuit.'" VLSI Opp. at 9. As evidence, VLSI cites to the Conte

Report, which states, "Each core includes performance measurement circuitry used for running various tests to measure the operational frequencies and corresponding voltages of each core. The performance measurement circuitry includes critical path monitoring circuitry for testing critical paths used for measuring such frequencies and voltages." Conte Report ¶ 339. VLSI also claims that Dr. Conte explains in his deposition that Intel meets the technical requirements of the "performance measurement circuit" limitation irrespective of any testing by Intel. VLSI Opp. at 9 (citing ECF No. 579-5 (Conte Dep.) 108:17–113:18). VLSI then claims that "Intel's reliance on [*INVT*], is misplaced because each Accused Product includes 'a performance measurement circuit for measuring a performance parameter value for said core.'" VLSI Opp. at 9 (citing Conte Report at ¶ 339). As a fallback, VLSI relies on its global stipulation, (which the Court has rejected, *see supra*).

The Court agrees with Intel. The claim limitation that the circuit is "for measuring" ('836 Patent at 11:20–23) points to "capability, as opposed to actual operation", so "an apparatus that is reasonably capable of performing the claimed functions without significant alterations can infringe those claims." *INVT*, 46 F.4th at 1375–76 (citations and quotations omitted). The question then is whether the accused technology is "reasonably capable" of performing the claimed functions. *Ibid.* VLSI has presented evidence that the accused technology contains a "performance measuring circuit" but puts forth no evidence that the accused technology is capable of "measuring a performance parameter" ('836 Patent at 11:20–23) except when used with ATE testers. *See* Conte Report ¶ 339 ("Intel uses an ATE tester as part of the test apparatus"). And, as discussed *supra*, VLSI has put forth no evidence that ATE testing is performed in the United States. When asked if the "performance measurement circuits can be used for measuring a performance parameter value when not connected to [an ATE] tester," Dr. Conte replied that he had not "opined one way or the other." ECF No. 579-5 (Conte Dep.) 111:4–112:24. Dr. Conte further admitted that he "had not sought any evidence" when asked whether "anyone actually has used the performance measurement circuit for measuring a performance parameter value when not connected to a tester." *Id.* Thus, there is no evidence that the accused technology is reasonably capable of meeting the testing claim limitation in the United States. Having found that VLSI's

evidence does not create a genuine dispute of material fact as to whether the testing limitation occurs in the United States, the Court finds as a matter of law that VLSI cannot prove that Intel infringes claims 10, 11, 13, and 17 of the '836 Patent. Thus, Intel's Motion for Summary Judgment of no infringement of claims 10, 11, 13, and 17 of the '836 Patent is granted.

2. Infringement of the '922 Patent

VLSI accuses Intel of infringing claims 4, 5, and 18 of the '922 Patent. Claim 1 (upon which claims 4 and 5 depend) recites, "A power island for a system-on-a-chip (SoC), the power island comprising: . . . a supply line to receive an ***external supply signal (VDD)***[.]" '922 Patent at 9:10–21 (emphasis added). Claim 4 further recites, "The power island of claim 1, further comprising a reference line to receive a ***reference signal (VSS)***[.]" *Id.* at 9:50–51 (emphasis added). Claim 5 further recites:

> The power island of claim 4, wherein:
>
> the supply power converter comprises a ***VDD*** switch with a first added resistance to cause a first voltage drop and reduce the supply voltage of the external supply signal to the second voltage of the second power characteristics; and
>
> the reference power converter comprises a ***VSS*** switch with a second added resistance to cause a second voltage drop and change the reference voltage consistent with the second power characteristics.

Id. at 9:62–10:4 (emphasis added). Claim 17 (upon which claim 18 depends) recites:

> A method for making a power island for a system-on-a-chip (SoC), the method comprising:
>
> coupling a memory device to a supply line of the power island, wherein the supply line is configured to receive an ***external supply signal (VDD)*** from an external power control to operate the memory device according to first power characteristics;

Id. at 11:41–12:5 (emphasis added). Claim 18 further recites:

> The method of claim 17, further comprising: coupling the logic . . . .
>
> coupling a reference power converter to the logic module, wherein the reference power converter is configured to change at least one power characteristic of a ***reference signal (VSS)*** to generate an internal reference signal (VSSi) according to the second power characteristics;

Id. at 12:19–27 (emphasis added).

Intel seeks summary judgment of no infringement because it argues that VLSI has failed "to identify anything in Intel's accused products that constitutes converting a 'VSS' reference signal—a requirement of each asserted claim." Intel Mot. at 8. Intel argues, and VLSI does not dispute, that VLSI technical expert Dr. William Henry Mangione-Smith accuses a signal called "VCCIN" (also called "Vcc" or "Vin") of meeting both the "external supply signal (VDD)" and "reference signal (VSS)" limitations. Intel Mot. at 8; ECF No. 579-10 ("Mangione-Smith Suppl. Report") ¶¶ 197–202, 207–16, 227–47; ECF No. 579-11 ("Mangione-Smith Dep.") 73:4–77:19, 94:11–95:13, 127:12–134:12. Intel makes two arguments as to why this supports a finding of no infringement. First, Intel makes a claim construction argument that the term "reference signal" is limited by the parenthetical term "VSS." Second, Intel argues that Dr. Mangione-Smith's theory is internally contradictory. The Court addresses the arguments in turn.

a. Whether "VSS" is an Express Claim Limitation

Intel's first argument is that "VSS" is an express claim term and therefore limits the type of "reference signal" to a particular type of signal, "VSS." Intel Mot. at 10.

"The mere fact that a limitation is placed within parentheses does not mean it is no longer a part of the claim." *Janssen Pharmaceutica, N.V. v. Eon Labs Mfg., Inc.*, 134 F. App'x 425, 428 (Fed. Cir. 2005). In *Janssen*, the Federal Circuit considered whether the claim language describing a sieve, "600 to about 700 μm (25–30 mesh)," was limited by the term "(25–30 mesh)" even though it was in parentheses. *Id.* at 428. The first part, "600 to about 700 μm," referred to dimensions of a sieve, and the parenthetical, "(25–30 mesh)," referred to the size of the bead cores, an additional characteristic of the sieve. *Id.* at 428–429. The court concluded that "one having ordinary skill in this art would interpret 'a diameter of from about 600 to 700 μm (25–30 mesh)' to describe cores 1) labeled 25–30 mesh at the time of manufacture and classification, and 2) having a particular diameter, about 600–700 μm." *Id.* The court further reasoned that if it were to "conclude that claim 1 simply covers all cores having a diameter 600–700 μm across the center [it] would be rendering the phrase '25–30 mesh' superfluous." *Id.* at 428.

Intel argues that "the stated purpose of the reference power converter is specifically to change 'VSS' by a certain amount purportedly to simplify communications within the power

island." Intel Mot. at 10; '922 Patent at 7:34–49; 7:57–8:7; Figure 4 (showing VSS being raised from 0.0V to 0.2V). Intel adds that the specification consistently describes using "VSS" as the reference signal—in every single embodiment. *E.g.*, '922 Patent at 5:10–17, 6:64–65, 7:50–54, 8:26–53 ("reference signal, VSS"); Figs. 1–7 (all describing the "reference signal" as "VSS"); ECF No. 579-14 ("Apsel Rebuttal Report") ¶¶ 55–60, 63–67, 144–167. Intel further notes that claim 5, which depends on claim 4, "specifically recites a 'VSS switch' as part of the 'reference power converter.'" '922 Patent at 10:1–4. Intel argues that claim 5's "switch" is a "***VSS*** switch" because "it switches the 'VSS' signal recited in claim 4," which "further confirm[s] that 'VSS' in claim 4 is limiting." Intel Mot. at 11.

VLSI responds that "Intel does not offer any evidence that a limiting 'VSS' would exclude the accused 'reference signal' or explain what it contends the term would mean." VLSI Opp. at 11. Rather, VLSI argues, the parenthetical in "reference signal (VSS)" refers to examples of the "reference signal" that are labeled "VSS" in the specification and figures, without incorporating every feature of these examples into the claims. VLSI Opp. at 11–12 (citing *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 2015 WL 6956722, at *5, *7 (E.D. Tex. Nov. 9, 2015), *Hochstein v. Microsoft Corp.*, 2009 WL 1838975, at *12–16 (E.D. Mich. June 22, 2009)). VLSI also puts forth a theory that "VSS" is a "reference character" and is thus "considered as having no effect on the scope of the claims." VLSI Opp. at 12 (quoting MPEP § 608.01(m)). As for the later instances of a non-parenthesized "VSS," VLSI argues that claim 5's "VSS switch" refers to one of two separately recited switches (the other a "VDD switch"), which VLSI argues its expert identifies separately. *See* Mangione-Smith Suppl. Report ¶¶ 249–57; ECF No. 579-12 (Mangione-Smith Reply Report) ¶¶ 160–62.

It is clear from the parties' discussion of this issue that infringement depends on further claim construction and the parties have adequately set out their respective positions. *General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 983 (Fed. Cir. 1997). Intel urges a construction that "reference signal (VSS)" is limited to a particular type of signal, VSS. Intel Mot. at 10. VLSI argues that (VSS) only refers to examples of the "reference signal" and is not limiting. VLSI Opp. at 11–12.

Intel persuasively argues that the term "reference signal" is limited by the term "(VSS)." The specification uses the term "reference signal" eight times, and seven of those times the term is accompanied with the term VSS. '922 Patent at 5:11 ("reference signal, VSS"), 5:13 (same), 5:16–17 (same), 6:64–65 (same), 7:52 (same), 8:45 (same), 8:52 (same), 6:59 ("reference voltage, VSS, of the reference signal"). Furthermore, if the term "VSS" did not limit "reference signal," "VSS" would be given no effect. *Janssen*, 134 F. App'x at 428; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) ("It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'"); *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous."); *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) ("[C]laims are interpreted with an eye toward giving effect to all terms in the claim."). And as Intel points out, "claim 5, which depends on claim 4, specifically recites a 'VSS switch' as part of the 'reference power converter'" which "further confirm[s] that 'VSS' in claim 4 is limiting." Intel Reply at 11.

VLSI's case law does not suggest a different outcome. In *NXP USA, Inc. v. Impinj, Inc.*, the court construed the term "specific useful data (n×UDB)" (where UDB means useful data blocks, n is the number of UDB, and n and UDB are multiplied together in the parenthetical) to mean "some, but not all, useful data (UD)." 2022 WL 16716226, at *8. VLSI contends that the *NXP* court found that the parenthetical "referred to examples . . . that are labeled . . . in the specification and figures, without incorporating every feature of these examples into the claims." VLSI Opp. at 11–12. The Court disagrees. In *NXP*, Impinj argued that "the inclusion of '(n×UDB)' in the claims refers only to specific useful data transmitted in response to a request." 2022 WL 16716226, at *9. But the court disagreed with Impinj, instead finding 1) it was "unclear whether the patent defines 'n×UDB' to refer only to requested data" and 2) the term "n×UDB" was used inconsistently throughout the patent. *Id.* at *10. The issue before this Court is distinguishable. Unlike the term "n×UDB," which was not fully defined and was used inconsistently, here, the term "VSS" has clear meaning to both parties (Mangione-Smith Dep. 139:3–141:6; Intel Reply at 7) and is used consistently throughout the patent ('922 Patent at 5:11,

5:13, 5:16–17, 6:59, 6:64–65, 7:52, 8:45, 8:52).

VLSI's argument that "VSS" is a reference character is also unavailing. MPEP 608.01(m) provides (emphasis added):

> When there are drawings, there shall be a brief description of the several views of the drawings and the ***detailed description of the invention shall refer to*** the different views by specifying the numbers of the figures, and to ***the different parts by use of reference letters or numerals*** (preferably the ***latter***).

VLSI contends that "VSS" is a reference character. But "VSS" is a well-known term with an understood meaning in the field, as Dr. Mangione-Smith acknowledges. Mangione-Smith Dep. 139:3–141:6. To use a well-known term discussed throughout the specification as a reference character would be an implausibly irresponsible way to label a circuit or prosecute a patent. *Core Wireless* and *Hochstein* are thus of no use to the Court because both concerned "reference characters" or "reference numbers" used to identify elements in patent drawings. *Core Wireless*, 2015 WL 6956722, at *5, *7 (addressing whether "reference numbers" were limiting); *Hochstein*, 2009 WL 1838975, at *12–16 (addressing whether reference characters "L1, L2" in the parenthetical "communication couplers (L1, L2)" were limiting).

Thus, the Court finds that the parenthetical term "(VSS)" limits the term "reference signal."

b. Infringement Under This Claim Construction

The issue now is whether this construction dooms VLSI's theory of infringement. Intel argues that Dr. Mangione-Smith's opinion that VDD and VSS are the same is problematic because, according to Intel, he admitted during deposition that VSS and VDD must be different. Intel Mot. at 9; Mangione-Smith Dep. 132:8–134:12, 135:6–11, 136:22–138:3, 172:23–173:6. Intel further argues that VDD and VSS cannot be the same because the '922 Patent describes VDD and VSS as different voltage signals. Intel Mot. at 9; '922 Patent at 2:16–30, 2:44–53, 5:63–67, 6:52–53, 8:26–53 ("external supply signal, VDD"); '922 Patent at 5:10–17, 6:64–65, 7:50–54, 8:26–53 ("reference signal, VSS"); '922 Patent, Figs. 1–6 (all depicting "VDD" as a separate voltage signal at the header of the power island and "VSS" as the voltage signal at the footer of the power island); *id.*, Fig. 4 (showing VDD as "1.0V" and VSS as "0.0V"); Apsel Rebuttal Report ¶¶

144–167.

In response, VLSI does not back away from its theory that VDD and VSS are the same voltage signal. VLSI Opp. at 9–11. Instead, VLSI argues that nothing in the claims prevents the "supply signal" from being the "reference signal." VLSI Mot. at 9–10 (citing *Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1231–32 (Fed. Cir. 2011)). VLSI further argues that Dr. Mangione-Smith left open in his deposition the possibility that VDD and VSS are the same voltage signal. *See e.g.*, *id.* ("that a POSA would 'generally' understand a voltage labeled VSS to 'likely not to be a higher voltage' than a voltage labeled VDD, which does not prevent them from being equal.") (quoting Mangione-Smith Dep. 135:6–11). VLSI also points to lengthy excerpts of the Mangione-Smith Suppl. Report ("identifying these signals") and Mangione-Smith Reply Report, which "respond[s] to Intel's supply and reference signal arguments." VLSI Opp. at 10–11 (citing Mangione-Smith Suppl. Report ¶¶ 196–203, 230–34, ECF No. 579-12 (Mangione-Smith Reply Report) ¶¶ 133–65).

The Court agrees with Intel. As an initial matter, the Court finds that the parties agree that Dr. Mangione-Smith's theory of infringement identifies a signal called VCCIN as meeting both the VDD and VSS limitations. *See* Mangione-Smith Suppl. Report ¶ 197 ("Intel documents show, for example, that the voltage supply to an internal voltage regulator, as denoted in some documents by symbols such as ***'Vccin,' 'Vcc,' and 'Vin', is an example of an external supply signal (VDD)"***) (emphasis added); *id.* ¶ 232 ("an Intel presentation on FIVR depicts a [redacted] block that receives a signal 'Vin' and produces an input to a 'DAC' block. This input to the [redacted] is an example of a reference line, and ***the signal 'Vin' is an example of a reference signal VSS***.") (emphasis added); Intel Mot. at 8; VLSI Opp. at 11.

VLSI's argument that the supply signal (VDD) and the reference signal (VSS) can be the same signal fails. VLSI points to additional examples and embodiments in "other parts of the specification not cited by Intel [that] contemplate signals provided by multiple sources in some embodiments and by a common source in others." VLSI Opp. at 10; *see, e.g.*, '922 Patent at 4:46–57 (embodiments where "supply signals" are generated by three sources or one source), 5:4–17 (stating that circuits may connect to "separate nodes of the same reference signal," "the same node

of a single reference signal," and "two or more distinct reference sources"). VLSI also claims that "there are embodiments in which voltages that are depicted as distinct in one of the patent's figures are nevertheless the same." VLSI Opp. at 10; '922 Patent at 4:49–55 (controls depicted as providing "different" supply signals in Figure 1 may in "other embodiments" provide signals "with the same or similar supply voltages"). These citations to the patent amount to little more than attorney argument and vague speculation, thus the Court finds that they are not probative evidence of infringement.

VLSI's argument that Dr. Mangione-Smith opined that VSS and VDD could be the same voltage signal also fails. Dr. Mangione-Smith testified at his deposition that VDD and VSS are generally different voltages:

> Q. Okay. Now, let's look back at the '922 Patent, at figure 2 again. There's a reference that we discussed earlier to VDD at the top; right?
> A. Yes.
> Q. And there's a reference to VSS at the bottom; correct?
> A. Yes, that's correct.
> Q. And those are using two different labels for two voltages; correct?
> A. Yes, that's correct.
> Q. You would expect them to be distinct; correct?
> A. Yes. ***Generally, unless, you know, the one exception would be if the VDD had a power gate that was turned off. But during operation, I would certainly expect them to be different voltages***.

Mangione-Smith Dep. 132:8–24 (emphasis added). Dr. Mangione-Smith also testified that the difference between VDD and VSS is generally defined as the voltage across a circuit:

> A. . . . Yeah, VDD is generally defined, relative to VSS.
> Q. And what do you mean by, "VDD is defined generally, relative to VSS"?
> A. Well, VDD is providing a voltage. What voltage? Voltage is always relative. So you know, if we've got something that we call 0 volts and we measure that this thing is 2 volts higher, we would call VDD 2 volts. That doesn't mean, in any absolute sense, there's 0 volts and 2 volts. It's all relative.
> Q. So VDD minus VSS is the voltage across the circuit; right?
> A. In general, yeah. As in most – you know, if a person of ordinary skill in the art saw a circuit with VDD and VSS, I think that they would go in with the assumptions that that was the voltage across the circuit, the difference between the two.

Mangione-Smith Dep. 137:2–20. VLSI tries to make the most of these statements by claiming that Dr. Mangione-Smith technically left open the possibility of VSS and VDD being the same. VLSI Opp. at 11 ("a POSA would 'generally' understand a voltage labeled VSS to 'likely not to

be a higher voltage' than a voltage labeled VDD, which does not prevent them from being equal") (quoting Mangione-Smith Dep. at 135:6–11). But this stretches his testimony too far. Dr. Mangione-Smith only presents one example where VDD and VSS would be the same, if "VDD had a power gate that was turned off" and he does not claim this situation as part of his theory of infringement. Mangione-Smith Dep. 132:8–24. Rather, Dr. Mangione-Smith states quite clearly that "during operation," he "would certainly expect [VSS and VDD] to be different voltages." *Id.*

VLSI's citation to *Powell* for the prospect that "the same features in the accused product satisfied two separately recited elements" also fails. VLSI Opp. at 10 (citing *Powell*, 663 F.3d 1221, 1231–32). In *Powell*, the Federal Circuit cited to a patent's specification for evidence that one component could meet two limitations. 663 F.3d at 1231 ("[T]he disclosure in the specification cuts against Home Depot's argument that the 'cutting box' and 'dust collection structure' must be separate components . . . . [The specification] does not suggest that the claim terms require separate structure"). Here, VLSI points to no such evidence from the specification or claims of the '922 Patent. Instead, all evidence, including the testimony of VLSI's own expert, suggests that VDD and VSS must be different.

Furthermore, the Court finds no probative evidence in VLSI's citations to the Mangione-Smith reports. VLSI Opp. at 10–11 (citing Mangione-Smith Suppl. Report ¶¶ 196–203, 230–34, ECF No. 579-12 (Mangione-Smith Reply Report) ¶¶ 133–65). The excerpts of Dr. Mangione Smith's supplemental report lay out only the infringement theory critiqued by Intel where VCCIN is both VSS and VDD. Mangione-Smith Suppl. Report ¶¶ 197, 232. VLSI points to no evidence of an alternative theory of infringement or an explanation that VSS and VDD can be the same voltage signal. Dr. Mangione Smith's reply report fares no better. The fifteen-page excerpt provided by VLSI in its opposition papers takes issue with Intel expert Dr. Apsel's claim construction of VSS, but does not put forth any affirmative infringement theory where the reference signal is VSS. *See, e.g.*, ECF No. 579-12 (Mangione-Smith Reply Report) ¶ 135 ("Dr. Apsel further states that the term reference as used in the '922 Patent is always and consistently used to mean VSS or ground . . . . I disagree.") (citations and quotations omitted); *id.* ¶ 140 ("I disagree with Dr. Apsel that the examples she cites provide support for her conclusions about the

meanings of 'VSS,' 'reference,' and 'ground.'"); *id.* ¶¶ 156–165 (opining that the term "VSS" in claim 4 is not limiting because it is in parentheses). The reply report excerpt is of no use here because it pertains to claim construction, which the Court addressed in the previous subsection.

All evidence (other than attorney argument and vague speculation) suggests that VDD and VSS are different voltage signals, which is at odds with Dr. Mangione-Smith's infringement theory that VCCIN satisfies both the VSS and VDD limitations. Mangione-Smith Suppl. Report ¶¶ 197, 232. Furthermore, VLSI put forth no other theory of infringement in its opposition. Thus, the Court finds that Intel has shown that an essential element of VLSI's infringement claim is missing, and that VLSI has therefore failed to put forth material evidence in support of a theory of infringement. The Court finds as a matter of law that VLSI cannot prove that Intel infringes the '922 Patent, so Intel's Motion for Summary Judgment of no infringement of the '922 Patent is granted.

3. Validity of the '922 Patent

Intel further contends that the Asserted Claims of the '922 Patent are invalid as indefinite as a matter of law because the patent "fails to provide persons of ordinary skill with information sufficient to determine with reasonable certainty when a component is a 'power island' and when it is not." Intel Mot. at 11.

"[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014); *see also Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1371 (Fed. Cir. 2015) ("[A] claim is indefinite if its language might mean several different things and no informed and confident choice is available among the contending definitions.") (citations and quotations omitted).

The Background section of the '922 Patent describes a "power island" as a group of components with "similar" power requirements:

> One power management design approach combines components with similar power requirements into groups, which are referred to as power islands or, in some instances, voltage islands. All of the

> ***components within a power island typically have similar power characteristics*** that are unique from the power characteristics of other power islands.

'922 Patent at 1:29–35 (emphasis added). The two independent Asserted Claims of the '922 Patent (claim 1 and claim 17) contain language describing components of a power island with power characteristics that are "different" or "partially different." Claim 1 reads:

> A ***power island*** for a system-on-a-chip (SoC), the power island comprising:
>
> a first segment comprising a hardware device, the first segment to operate the hardware device at first power characteristics indicative of at least a first voltage;
>
> a second segment comprising scalable logic, the second segment to operate the scalable logic at second power characteristics indicative of at least a second voltage, wherein the second power characteristics of the scalable logic ***are different*** from the first power characteristics of the hardware device; . . .

'922 Patent at 9:9–20 (claim 1) (emphasis added). Claim 17 reads:

> A method for making a ***power island*** for a system-on-a-chip (SoC), the method comprising:
>
> coupling a memory device to a supply line of the ***power island***, wherein the supply line is configured to receive an external supply signal (VDD) from an external power control to operate the memory device according to first power characteristics;
>
> coupling a supply power converter to the supply line of the ***power island***, wherein the supply power converter is configured to change at least one power characteristic of the external supply signal to supply an internal supply signal (VDDi) to a logic module on the ***power island*** according to second power characteristics ***that are at least partially different*** from the first power characteristics; . . .

Id. at 11:41–12:13 (claim 17) (emphasis added).

Intel argues that the claims are indefinite because they describe power islands with the contradictory terms of degree "similar," "different," and "partially different." Intel first argues that the specification "suggests that the existence of a 'power island' turns on the degree of similarity between the 'power characteristics' of components—without providing any information about how to determine when a component is sufficiently 'similar' in that respect to qualify as a

'power island.'" Intel Mot. at 12. Intel then argues that the claim language of the Asserted Claims "impos[es] another degree-based standard, but in the opposite direction—by requiring certain components within the 'power island' to have 'power characteristics' that are 'different' (claim 1, from which claims 4 and 5 depend) or "partially different" (claim 17, from which claim 18 depends) from the "power characteristics" of other components within the 'power island.'" *Id.* (citing '922 Patent). Intel adds that first-named inventor David Evoy's testimony shows that the term is indefinite because he could not identify objective boundaries for the term "power island" but instead "confirmed none exists." Intel Mot. at 13.

Intel cites three cases with indefiniteness arguments comparable to those in the instant case. In *Varian Med. Sys., Inc. v. ViewRay, Inc.*, the court found that a claim for a medical device requiring "substantially the same" and "different" cross sections was indefinite where "the specification does not contain objective guidance to inform a POSITA regarding what cross sections would qualify as 'substantially same' or 'different.'" No. 19-cv-05697-SI, 2020 WL 4260714, at *6–7 (N.D. Cal. July 24, 2020). In *ACQIS LLC v. Alcatel-Lucent USA Inc.*, the court found that the term "similar in design" in a computer system patent was indefinite where plaintiff "was unable to articulate any point at which components or circuitry would cease to be 'similar'" and "the claims fail[ed] to 'provide objective boundaries for those of skill in the art.'" No. 6:13-cv-638, 2015 WL 1737853, at *10 (E.D. Tex. Apr. 13, 2015). And in *Power Integrations, Inc. v. ON Semiconductor Corp.*, the court found that a "moderate power level" in power supply circuit patent was indefinite where the specification failed to "provide some meaningful way to determine what the moderate value is." No. 16-cv-06371-BLF, 2018 WL 5603631, at *20 (N.D. Cal. Oct. 26, 2018)

VLSI responds with several arguments. First, VLSI argues that "the preamble term 'power island' is not a limitation in the asserted claims" because the term appears only in the preamble of claim 1. VLSI Opp. at 12–13. Rather, VLSI asserts that its "expert confirms, a 'power island' in the sense of claim 1 is simply a system having the components that are recited in the body of claim 1: a structurally complete invention." *Id.* (citing ECF No. 617-11 (Mangione-Smith Reply Report) ¶¶ 100–13). Second, VLSI contends that Intel's arguments "erroneously presume that the claim

preambles incorporate aspects of the 'Background' section as limitations" and noted that none of Intel's cases address preamble language. *Id.* at 13. Third, VLSI argues that Intel waived its indefiniteness argument. *Id.* Finally, VLSI counters Mr. Evoy's deposition testimony about the breadth of the term power island by countering that its own expert has shown that the accused products contain "power islands" under the plain and ordinary meaning of the term. *Id.* at 12–13 (citing ECF No. 617-11 (Mangione-Smith Reply Report) ¶¶ 171–78).

Intel replies that the term "power island" is limiting because "every asserted claim contains one or more non-preamble limitations directed to 'the power island.'" Intel Reply at 8–9. Intel also points to evidence that it reserved its right at *Markman* to make an indefiniteness argument at summary judgment and disclosed indefiniteness theories in its contentions. *Id.* at 9.

The Court first addresses VLSI's waiver argument. Intel provides several examples in its reply papers showing that it disclosed the indefiniteness argument currently before the Court. For example, Intel stated in its Invalidity Contentions:

> All asserted claims of the '922 patent . . . are invalid under 35 U.S.C. 112. . . . For example, the specification states that "power islands" can mean "components with similar power requirements" and that power islands "typically have similar power characteristics that are unique from the power characteristics of other power islands" '922 patent at 1:20–35. However, claim 1 and its dependents also require segments within the power island must have different power characteristics from one another.

ECF No. 710-10 (3/19/18 Contentions) at 1594–95; ECF No. 710-11 (1/26/22 Contentions) at 1377 (same); Apsel Report ¶ 1181; Apsel Reply Report ¶ 666. Furthermore, Intel stated in its *Markman* briefing that "Intel may raise at a later time . . . such as in an authorized Motion for Summary Judgment[] any indefiniteness arguments as to th[at] term[]." ECF No. 106. The Court finds that Intel's disclosures and explicit reservation of rights show that Intel did not waive its indefiniteness argument.

VLSI's argument that the term "power island" is not limiting also fails. Preamble language is not limiting "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 770 (Fed. Cir. 2018) (quoting

Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002)). But "[w]hen limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003). Here, the remaining claims rely on the antecedent basis from the preamble. *See, e.g.*, '922 Patent at 9:53 (claim 4) ("the power island"), 12:7 (claim 17) (same). Thus, the Court finds that the term "power island" is limiting.

Having found that Intel has not waived its indefiniteness argument and that the term "power island" is limiting, the Court turns to the substance of the parties' indefiniteness arguments. Again, the Court agrees with Intel. VLSI does not provide, and the Court cannot find, any objective guidance or boundaries in the patent that persons of ordinary skill could use to determine with reasonable certainty when "power characteristics" are "different" and "partially different"—yet at the same time sufficiently "similar"—to be within the claimed "power island." Other than its preamble argument (VLSI Opp. at 13), which the Court has rejected, VLSI has made no effort to distinguish Intel's cases. The Court is particularly persuaded by *Varian*, where the court found that claims describing cross-sections of "leaves" used in radiotherapy as "substantially the same" and "different" were indefinite despite "some examples" in the specification "of what could be considered 'substantially same' and 'different'" and expert testimony "that a 1-3 percent difference in leaf width would qualify as 'substantially same' while a 20-50% in leaf width would not" because the specification "[did] not disclose any dimensions, angles, or position of radiation source." 2020 WL 4260714, at *6–7.

Here, VLSI similarly points to nothing in the specification describing power characteristics in a way that gives any objective meaning to the words "similar," "different," and "partially different." VLSI's only purported evidence is eight paragraphs of the Mangione-Smith Reply Report, where VLSI argues that its expert "has shown that the accused products contain 'power islands' under the plain and ordinary meaning of the term." VLSI Opp. at 15. Much of this excerpt is concerned with which components belong in a power island, not the power characteristics within the power island. *See, e.g.*, Mangione-Smith Reply Report ¶ 171 ("To the

extent that Dr. Apsel believes that two components cannot be part of a 'group of components with similar power requirements' if they are supplied by different FIVRs, I disagree"); *id.* at ¶ 175 ("I do not understand how evidence that might be cited in support of a conclusion that the accused PCU, L3 cache/LLC, and cores are part of the same 'power island' constitutes a 'theory' that ***excludes*** other things . . . from being parts of the same 'power island.'") (emphasis in original). The final paragraph discusses power characteristics and lists the terms "similar," "different," and "partially different," but does not attempt to define their boundaries. *Id.* at ¶ 178 ("the definition of power island does not preclude groups of components with partially different or different power characteristics if those characteristics would be considered similar by one of ordinary skill in the art.") (quoting IPR2018-01144, Paper No. 32 (Final Written Decision) at 77, 79). Contrary to what VLSI's briefing claims, the Court cannot identify any explanation from Dr. Mangione-Smith's Reply Report about how the power island is understood under the plain and ordinary meaning of the term. More importantly, the report supplies no evidence of objective boundaries or guidance on the scope of the power characteristics within a power island that explains what "similar," "different," and "partially different" mean. Thus, the Court finds that a person of ordinary skill, looking to the specification and the prosecution history, could not with reasonable certainty determine the scope of the claim. *Nautilus*, 572 U.S. at 910.

The Court is also persuaded by testimony of the first-named inventor, David Evoy. "[I]nventor testimony" is "evidence [that] may be helpful to explain . . . the meaning of technical terms, and terms of art." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996). Mr. Evoy testified that the meaning of "power island" may be "a quite fluid definition," Evoy Dep. 96:4–17, "could change depending on the context of a meeting and who was there," *id.* at 97:23–98:1, and "might even depend [on] who is sitting across the table from me," *id.* at 96:14–17. So boundless was the term to him that he could not say whether "[w]ithin the context of power management, maybe Manhattan could be a power island." *Id.* at 82:22–24. While the deposition testimony is secondary in the Court's determination, the Court finds that Mr. Evoy's inability to identify objective boundaries for the term "power island" further suggests that the claims are indefinite.

Where Intel has put forth evidence from the specification and the inventor that the term "power island" is indefinite, VLSI has put forth no material evidence to the contrary. Intel has shown, as a matter of law, that the '922 Patent is indefinite. Thus, Intel's Motion for Summary Judgment that the '922 Patent is invalid as indefinite is granted.

4. Infringement of the '806 Patent

VLSI accuses Intel of infringing claims 11, 12, 13, and 15 of the '806 Patent. Intel Mot. at 13. The claims all require a "first memory" and a "second memory," and two different modes of operation, "a first mode of operation" and "a second mode of operation." '806 Patent at 10:31–57. The Court construed "second mode of operation" to require that, "when in the second mode of operation, both the voltage provided to the first memory and the voltage provided to the second memory must be lower than the minimum operating voltage of the first memory." Markman Order at 7.

Dr. Conte describes VLSI's theory of infringement. According to Dr. Conte, a circuit component called a sleep transistor [redacted]. For the first mode of operation, when a memory is being read from or written to, the sleep transistor [redacted] Conte Report ¶¶ 807, 874; ECF No. 678-14 at 2. For the second mode of operation, when the memory is not being read from or written to, on the other hand, the sleep transistor [redacted] Conte Report ¶¶ 806, 874; ECF No. 678-14 (Bendt Dep.) 76:13–77:11; ECF No. 678-5 (Conte Dep.) 191:6–23.

Intel makes two arguments. First, Intel argues that "VLSI and Dr. Conte have failed to identify ***any*** 'minimum operating voltage' for the data array memory in Intel's products accused as the claimed 'first memory.'" Intel Mot. at 15. Intel further contends that "Dr. Conte's opinion that a minimum operating voltage exists for each of the numerous individual bitcells within the

accused data array memory" does not address the claim limitation. *Id.*

VLSI responds that Dr. Conte concluded that "when the accused products are in the second mode of operation, 'the voltages supplied to the LLC data array [(the first memory of claim 11)] and the DCU state arrays [(the second memory of claim 11)], respectively, are lower than the minimum necessary for the first mode of operation.'" VLSI Opp. at 15 (citing Conte Report ¶ 941). VLSI argues that there is no need to quantify the minimum operating voltage to meet either the claims or the Court's construction. *Id.*

On this first point, the Court agrees with VLSI. The Court construed the term "second mode of operation" to have its "[p]lain and ordinary meaning, which includes the requirement of claim 11 that when in the second mode of operation the voltage(s) supplied to the first and second memory, respectively, must be lower than the minimum necessary for the first mode of operation." Markman Order at 6. A recitation of specific voltages is not required to meet the claim limitations as long as the voltage "when in the second mode of operation" is lower than "the minimum necessary for the first mode of operation." *Id.*

Second, Intel argues that Dr. Conte's Report does not show the difference in voltages because it improperly focuses on the minimum operating voltages of bitcells. Intel Mot. at 14–15. Intel argues that "Dr. Conte does not allege that the purported minimum operating voltage of a bitcell is the same as the minimum operating voltage of the data array memory; instead, he concedes that the data array memory can operate at voltages "even below" the bitcells' minimum operating voltage." *Id.* at 14 (citing Conte Reply Report ¶ 758); *see also* ECF No. 579-5 (Conte Dep.) 224:15–18 ("[T]he array can have a different, slightly different minimum operating voltage from the first memory cell topology or the second memory cell topology of the memory cells.").

VLSI responds with evidence that in both modes of operation, the DCU state array, the "second memory" of claim 11, is able to read and write, but when in the second mode of operation, the DCU state array receives a voltage lower than the minimum required to read and write the LLC memory array. Conte Report ¶¶ 940–51; Conte Reply Report ¶¶ 742–49.

The Court finds the Dr. Conte's report provides sufficient evidence to survive summary judgment. Dr. Conte concludes that "the voltages supplied to the LLC data array and the DCU

state arrays, respectively, are lower than the minimum necessary for the first mode of operation" because "the minimum operating voltage of the DCU state array bitcells is lower than the minimum operating voltage of the LLC data array in each of the '806 Accused Products." Conte Report ¶ 943. Drawing all inferences in VLSI's favor, the Court finds that Dr. Conte's reports and deposition testimony create a genuine dispute of material fact as to whether Intel infringes the '806 Patent. Thus, Intel's Motion for Summary Judgment of no infringement of the '806 Patent is denied.

5. Infringement of the '672 Patent

The sole asserted claim of the '672 Patent is directed to a chip-assembly process that includes a step whereby a "solder composition is provided as a fluid layer on the underbump metallization, which layer makes a contact angle of less than 90° with the underbump metallization." '672 Patent at claim 2.

VLSI accuses two Intel assembly processes, the relevant steps of which are undisputed: (1) a "Current Process" (used since [redacted]), in which Intel [redacted] onto what VLSI accused as the claimed "underbump metallization"; and (2) a "Discontinued Process" (not used since [redacted]), in which Intel [redacted] onto the accused underbump metallization. ECF No. 579-15 ("Neikirk Report") ¶¶ 140, 148–49, 153; Intel Mot. at 16.

Intel argues that the Court should grant summary judgment of no infringement "because there is no genuine dispute of material fact that (1) in the Current Process, solder is 'provided' [redacted], and (2) in the Discontinued Process, the contact angle between the solder composition and the accused underbump metallization was not 'less than 90°.'" Intel Mot. at 15–16. The Court addresses the two processes in turn.

a. Current Process

The Current Process (used since [redacted]), uses [redacted]. Intel Mot. at 16. Intel argues that this [redacted], and that VLSI expert Dr. Dan P. Neikirk is not accusing [redacted] as "provid[ing] solder as a fluid layer." ECF No. 579-16 ("Neikirk Dep.") 151:3–52:3. Thus, says Intel, the Current Process does

not infringe "because claim 2 requires that the solder composition be 'provided as a fluid layer,' and because it is undisputed that [the Current Process] instead [redacted]." Intel Mot. at 16–17.

VLSI disputes Intel's definition of the term "provided." VLSI Opp. at 19. VLSI cites to testimony of its expert Dr. Neikirk, who said that Intel "does not explain why, if 'providing' a solder composition had been intended to be limited to initial application of solder, the drafters of the '672 Patent chose to use the broader term 'providing' instead, and to make no reference to the step being 'initial' or being onto a surface that previously was solder-free." ECF No. 678-19 ("Neikirk Reply Report") ¶ 58. VLSI argues that contrary to Intel's assertion, the '672 Patent specifically emphasizes that "the solder [] can be applied in different manners." '672 Patent at 2:7–8. Dr. Neikirk further opines that a POSA would understand the plain meaning of "provide" to encompass making available or supplying. *See, e.g.*, ECF No. 677-23 (Merriam-Webster definitions of provided) ("to supply or make available; to make something available to"); ECF No. 677-24 (Dictionary.com definitions of provided) ("to make available"); ECF No. 677-25 (Collins dictionary definitions of provided) ("to make available; supply"); Neikirk Reply Report ¶ 57.

The Court has not construed the terms "provided" or "provided as," and the Parties' have not provided sufficient briefing for the Court to construe the claims here. As such, the Court applies VLSI's construction for summary judgment only. Dr. Neikirk has testified that the "current process involves fluid solder attaching to the accused underbump metallizations . . . happens [redacted]." Neikirk Report ¶¶ 204, 247 (citing witness testimony). Given VLSI's construction, Dr. Neikirk's testimony creates a genuine dispute of material fact as to whether the Current Process infringes the '672 Patent.

b. Discontinued Process

The Discontinued Process (not used since [redacted]), requires [redacted] onto the accused underbump metallization. Neikirk Report ¶¶ 140, 148–49, 153. Intel argues that the Discontinued Process does not infringe claim 2 because "VLSI has no evidence that any contact angle between [redacted] and the accused

underbump metallization is less than 90°, as required by claim 2" nor has VLSI "identified any measurement of any contact angle in any Intel accused product." Intel Mot. at 17.

VLSI responds with "extensive expert evidence" that the angle is less than 90°. VLSI Opp. at 19 (citing Neikirk Report ¶¶ 249–57, Neikirk Reply Report ¶¶ 59–62). VLSI also cites to documents and images suggesting that [redacted]. *See* Neikirk Reply Report ¶ 61; Neikirk Report ¶¶ 252–55 (collecting Intel evidence).

The Court finds that VLSI's evidence creates a genuine dispute of material fact as to whether the Discontinued Process infringes the '672 Patent. Thus, Intel's Motion for Summary Judgment of no infringement of the '672 Patent is denied.

6. License Defense

As discussed at Section III.A.1, the Court will issue a supplemental order regarding Intel's license defense.

7. Willful Infringement, Indirect Infringement, and Enhanced Damages

Intel seeks summary judgment that any infringement was not willful or indirect because it had no knowledge of the Asserted Patents, much less any knowledge of infringement.

Indirect and willful infringement both require proof, for each asserted patent, that the defendant knew or should have known (1) of the patent, and (2) that it was infringing the patent. *See Commil USA, LLC v. Cisco Sys., Inc.*, 575 U.S. 632, 639 (2015) (indirect infringement "requires knowledge of the patent in suit and knowledge of patent infringement"); *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1371 (Fed. Cir. 2017) (same for willful infringement); *Sonos, Inc. v. Google LLC*, 591 F. Supp. 3d 638, 647 (N.D. Cal. 2022) ("Like willful infringement, both forms of indirect infringement—induced and contributory infringement—require knowledge of the patent and knowledge of infringement."). There is no "per se rule" under which district courts evaluate willfulness contentions; rather, the factfinder must look to the "'totality of the circumstances presented in the case.'" *WCM Industries v. IPS Corp.*, 721 F. App'x 959, 970 (Fed. Cir. 2018) (quoting *Shiley, Inc. v. Bentley Labs., Inc.*, 794 F.2d 1561, 1568 (Fed. Cir. 1986)).

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a. Pre-Suit Knowledge

Some evidence of pre-suit knowledge put forth by VLSI pertains to all four of the Asserted Patents, and the remaining evidence pertains only to the '836 Patent. The Court first considers evidence pertaining to all the Asserted Patents to make a determination for the '806, '922, and '672 Patents, then the Court considers additional evidence pertaining only to the '836 Patent.

i. '806, '922, and '672 Patents

Intel argues that for three of the asserted patents (the '806, '922, and '672 Patents), VLSI failed even to allege pre-suit knowledge by Intel in its complaint, interrogatory responses, or contentions. Intel Mot. at 21–22; Compl. ¶¶ 47–49, 92–94, 120–22; ECF No. 580-41 (VLSI's Supplemental Response to Intel's 3rd Set of Interrogatories, "Interrog. Resp.") at 8–10; ECF No. 407-2 (VLSI's Second Amend. Infringement Contentions) at 15–17; ECF No. 477-3 (VLSI's Fifth Suppl. Damages Contentions) at 216–218.

VLSI does not address Intel's waiver argument, but instead responds with evidence that purportedly shows that "Intel regularly monitors competitors' (including NXP's) activities, and has acknowledged its competitors have patents covering similar products." VLSI Opp. at 23; *see, e.g.*, ECF No. 677-28 ("Intel 2012 10-K") at 17 ("Established competitors . . . as well as companies that purchase and enforce patents and other IP, may already have patents covering similar products."); ECF No. 677-29 ("Intel Datasheet") at -574 ("[T]he I^2C bus/protocol may require licenses from various entities, including NXP[.]"). VLSI also cites to evidence that "Intel has a policy discouraging engineers from looking at third-party patents" in support of a willful blindness theory including deposition testimony by Intel engineers and a 2006 book written by a former Intel executive. VLSI Opp. at 23–24 (citing ECF No. 678-10 ("Therien 30(b)(6) Dep.") 394:20–396:21, ECF No. 678-21 ("Chen Dep.") 12:10–13:11, ECF No. 677-32 ("*The Pentium Chronicles*") at 161 & n.3).

Intel replies that VLSI's argument that Intel monitors competitors "is (1) waived because VLSI did not raise it in its complaint or contentions, and (2) irrelevant and misleading given that VLSI admits that it has not identified any competitor products that supposedly practice the asserted patents, including those of NXP." Intel Reply at 14. Intel adds that its "engineers merely

explained their practice not to look at others' patents (to avoid being 'influenced'), and instead focused on their own 'innovations.'" *Id.* at 14–15 (citing Chen Dep. 12:10–13:11, Therien 30(b)(6) Dep. 394:20–396:21).

As an initial matter, the Court agrees with Intel that VLSI failed to disclose and has thus waived any argument that Intel had either knowledge of or knowledge of infringement of the '806, '922, and '672 Patents. Intel's Interrogatory No. 19 states:

> State the facts and Identify all Documents on which VLSI bases its allegation that Intel has willfully infringed the Asserted Patents, including by Identifying each instance in which VLSI has given notice to Intel of any alleged infringement and the specific content of such notice.

Interrog. Resp. at 7–8. VLSI's response, dated February 24, 2023, includes several general allegations pertaining to the Asserted Patents. *See, e.g.*, *id.* at 8 ("Intel has willfully infringed the Asserted Patents and continues to willfully infringe them. VLSI expects to seek enhanced damages as a result of the totality of the circumstances, including, among other things, Intel's willful infringement of the Asserted Patents."). Of the four remaining Asserted Patents, the only specific fact or document disclosed pertains to the '836 Patent, which Intel cited "during the prosecution of U.S. Patent No. 9,317,342" and "U.S. Patent No. 9,582,287." *Id.* at 10; '342 File History. VLSI made no disclosure of the Intel 2012 10-K, the Intel Datasheet, or the book *The Pentium Chronicles*, and did not cite to deposition evidence despite both depositions being taken before VLSI's response. Therien 30(b)(6) Dep. (taken on January 27, 2023); Chen Dep. (taken on February 8, 2023); VLSI's Supplemental Response to Intel's 3rd Set of Interrogatories (signed on February 24, 2023). Thus, the Court finds that VLSI has waived any argument related to knowledge of or knowledge of infringement of the '806, '922, and '672 Patents.

Even if VLSI's evidence pertaining to the Asserted Patents is not waived, the evidence is not significantly probative, and thus does not create a genuine dispute of material fact in support of pre-suit willful or indirect infringement of the Asserted Patents. The Court addresses VLSI's evidence: the Intel 2012 10-K, the Intel Datasheet, and the depositions and book (the Court addresses evidence specific to the '836 Patent in the next subsection).

The first piece of evidence is the Intel 2012 10-K for the end of fiscal year 2012, which

states:

> Established competitors in existing and new industries, as well as companies that purchase and enforce patents and other IP, may already have patents covering similar products. There is no assurance that we will be able to obtain patents covering our own products, or that we will be able to obtain licenses from other companies on favorable terms or at all.

Intel 2012 10-K at 17. The Court finds that this disclosure is not probative evidence of knowledge of the Asserted Patents. This is an ordinary corporate disclosure warning investors of the risks of patent litigation. If Intel had not made this disclosure, it could just as easily face securities litigation for failing to warn investors of the ever-present risk of patent litigation. And without any specific mention of the Asserted Patents, or any connection or mention of the accused technology, the Intel 2012 10-K is not material evidence of knowledge of the Asserted Patents, much less knowledge of infringement of the Asserted Patents.

VLSI's second piece of evidence is an Intel Datasheet, which states, "I^2C ls a two-wire communications bus/protocol developed by NXP. SMBus is a subset of the I2C bus/protocol and was developed by Intel. Implementations of the I2C bus/protocol may require licenses from various entities, including NXP Semiconductors N.V." Intel Datasheet at 89607DOC00025574. The Court finds that this is evidence of Intel's general knowledge of the NXP patent portfolio and knowledge of a risk of infringement of the NXP patent portfolio. But without any specific mention of the Asserted Patents, or any connection between the technology described in the datasheet and the accused technology, the Intel Datasheet is not material evidence of knowledge of infringement of the Asserted Patents .

VLSI's final set of evidence involves its claim that Intel is "willfully blind to risks of patent infringement." VLSI Opp. at 23. As an initial matter, the Court is concerned that this willful blindness theory is at odds with the theory VLSI puts forth ten lines earlier in its brief that "Intel regularly monitors competitors' (including NXP's) activities." *Id.*

Potential contradictions aside, the deposition and book excerpt are not material evidence of a corporate culture of willful blindness. For example, Tim Chen stated in his deposition that he is "not aware of any policy" at Intel not to look at patents of other companies. Chen Dep. 12:10–

13:11. In his deposition, Guy Therien states that it is discouraged, but "not a prohibited policy" to look at other patents. Therien 30(b)(6) Dep. 394:20–396:21. Therien explains:

> Generally, it's discouraged by Intel for their technical folks to look at other companies' patents, but it's not a prohibited policy. Like, they say that you can obviously look at it. It's, you know, any kind of offense to Intel's rules.
>
> So there's times when you'll see something come up from a colleague where they'll say, hey, look at this patent. You know, we already have a patent on that. Don't you think -- you know, things like that. So there will be that kind of discussion, especially when you have a lot of patents. And then there also will be times when counsel will bring specific patents to my attention to see if I'm -- of a consultive nature to see if --you know, some conversation about it. So those are the situations where I would see patents from other companies.

Id. 394:20–395:12. The Court finds that this evidence does not support VLSI's theory of willful blindness because both engineers testified that Intel has no policy restricting its engineers from looking at other companies' patents.

As a third piece of evidence of willful blindness, VLSI cites the 2006 book *The Pentium Chronicles*, written by Robert Colwell, Intel's former chief architect. The cited footnote states, "It is common practice in the industry to instruct engineers never to read the patents of other companies, a direction they universally comply with most happily. This helps avoid possible triple damages for 'willful infringement' if one's company is ever found to be infringing on another's patent." *The Pentium Chronicles*. The Court finds that this citation is not material evidence in support of VLSI's willful infringement allegation. First, the book was published in 2006 and VLSI presents no evidence that this "common practice" was ever an official policy at Intel during the period of alleged infringement (in fact, the deposition testimony refutes any inference that it was or still is). Furthermore, the book discusses potential patent infringement related to the P6 microprocessor, and VLSI draws no connection from that technology to the Asserted Patents or any accused technology. Finally, this is at best a general statement about Colwell's opinion about how the industry operates (circa 2006), not a clear statement that Intel practiced this policy. As such, the Court finds that this is not material evidence of knowledge of the Asserted Patents, knowledge of infringement of the Asserted Patents, or of willful blindness to the Asserted Patents.

VLSI has put forth several pieces of evidence that are unrelated, tenuous, and not significantly probative, perhaps in the hope that in combination they are equivalent to a single piece of material evidence. But VLSI's evidence is just as weak when viewed collectively under the totality of the circumstances as it is individually. Only the Intel Datasheet is evidence of a general knowledge of the NXP patent portfolio. And none of VLSI's evidence indicates knowledge of infringement of the Asserted Patents.

Having found that VLSI waived its argument that Intel had pre-suit knowledge and knowledge of infringement of the '806, '922, and '672 Patents, and that even if it hadn't, VLSI's evidence does not create a genuine dispute of material fact as to whether Intel had pre-suit knowledge of infringement of the '806, '922, and '672 Patents, the Court finds as a matter of law that VLSI cannot prove pre-suit willful or indirect infringement of the '806, '922, and '672 Patents by Intel. Thus, Intel's Motion for Summary Judgment of no pre-suit willful or indirect infringement of the '806, '922, and '672 Patents is granted.

ii. '836 Patent

For the reasons described above, the Intel 2012 10-K, the Intel Datasheet, and the depositions and book excerpt similarly do not create a genuine dispute of material fact relating to pre-suit willful or indirect infringement of the '836 Patent. The Court addresses a final piece of evidence directed towards only the '836 Patent, a citation to the '836 Patent in the prosecution of a subsequent Intel patent.

Intel argues that "VLSI only has alleged pre-suit knowledge because 'a patent examiner cited the application that led to the '836 Patent' during prosecution of two other patents." Intel Mot. at 22 (citing Interrog. Resp. at 10). Intel argues that "the undisputed facts also demonstrate that Intel did not have the requisite 'knowledge of infringement.'" Intel Mot. at 23 (quoting *Dali Wireless, Inc. v. Corning Optical Commc'ns LLC*, 638 F. Supp. 3d 1088, 1099 (N.D. Cal. 2022)). VLSI responds with evidence that Intel was aware of the '836 Patent because it cited the patent's application during prosecution. ECF No. 677-30 ("'342 File History") at 8, 11, 13, 16–26. Intel replies that VLSI has at most put forth evidence of "pre-suit knowledge of that patent" which it argues is "irrelevant to VLSI's burden to prove that Intel knew it infringed that patent." Intel

Reply at 14.

The Court agrees with Intel. VLSI's only authority on the matter found that "even substantive references to patents in the alleged infringer's patent prosecutions, without more, fail to sufficiently allege knowledge of infringement." *MasterObjects, Inc. v. Amazon.com, Inc.*, No. C 20-08103 WHA, 2021 WL 4685306, at *5 (N.D. Cal. Oct. 7, 2021). The Court follows *MasterObjects* and concludes that the '342 File History citation is at best evidence of knowledge of the patent, but is not evidence of knowledge of infringement.

Having found that VLSI's evidence does not create a genuine dispute of material fact as to whether Intel had pre-suit knowledge of infringement of the '836 Patent, the Court finds as a matter of law that VLSI cannot prove pre-suit willful or indirect infringement of the '836 Patent by Intel. Thus, Intel's Motion for Summary Judgment of no pre-suit willful or indirect infringement of the '836 Patent is granted.

b. Post-Suit Knowledge

Intel also seeks summary judgment of no willful infringement and no indirect infringement for the post-suit period. The issue here is not a dispute of evidence but rather of law. Intel argues that a Complaint does not provide "requisite knowledge of the patents" required for willful or indirect infringement. Intel Mot. at 22. VLSI responds that the Complaint, infringement contentions, and refinements to those contentions provided further evidence of infringement and cites to several cases where "post-filing conduct alone" support a theory of willful infringement. VLSI Opp. at 24.

The cases cited by the parties show a split among district courts as to whether a complaint provides adequate notice of willful and indirect infringement. Some courts have held that "a well-pled, detailed complaint laying out a clear case of infringement could supply the knowledge (post-complaint) required for willfulness once a defendant has had a reasonable period of time to evaluate the complaint's contentions[.]" *Dali*, 638 F. Supp. 3d at 1099 (quotation omitted); *see also PersonalWeb Techs. LLC v. Int'l Bus. Machines Corp.*, No. 16-CV-01266-EJD, 2017 WL 2180980, at *21 (N.D. Cal. May 18, 2017) (finding that a dispute between the parties as to whether the defendant's "noninfringement and invalidity defenses . . . are reasonable" precluded a

finding at summary judgment of no willful infringement). Other courts have held (at the pleadings stage) that a complaint alone is not sufficient to allege post-suit infringement. *See Sonos*, 591 F. Supp. 3d at 648 ("[W]ithout a notice letter or circumstances like the examples described previously, the complaint will generally not be adequate to serve as notice for either willful or indirect infringement."); *Splunk Inc. v. Cribl, Inc.*, No. C22-07611 WHA, 2023 WL 2562875, at *2–4 (N.D. Cal. Mar. 17, 2023) (similar); *ZapFraud, Inc. v. Barracuda Networks, Inc.*, 528 F. Supp. 3d 247, 250 (D. Del. 2021) ("[T]he complaint itself cannot be the source of the knowledge required to sustain claims of induced infringement and willfulness-based enhanced damages."); *VLSI Tech. LLC v. Intel Corp.*, 2019 WL 1349468, at *2 (D. Del. Mar. 26, 2019) (dismissing willfulness-based enhanced damages claim where the plaintiff had alleged that the defendant gained "knowledge of the [patent] at least since the filing of this complaint").

On this, the Court agrees with Intel. "The purpose of a complaint is to obtain relief from an existing claim and not to create a claim." *ZapFraud*, 528 F. Supp. 3d at 251; *Sonos*, 591 F. Supp. 3d at 648. Furthermore, because a complaint and infringement contentions are a necessary part of patent litigation, a finding that they alone satisfy post-suit notice would invite claims of willful infringement and indirect infringement into literally every patent suit. The Court has found that VLSI's only evidence of pre-suit infringement was knowledge of the '836 Patent, and VLSI's only evidence of post-suit notice is its complaint and infringement contentions. Thus, VLSI's evidence does not create a genuine dispute of material fact that would preclude summary judgment of no willful or indirect infringement. The Court finds as a matter of law that VLSI cannot prove post-suit willful or indirect infringement of the Asserted Patents by Intel. Thus, Intel's Motion for Summary Judgment of no post-suit willful or indirect infringement is granted.

c. Enhanced Damages

Under 35 U.S.C. § 284, in a case of infringement, courts "may increase the damages up to three times the amount found or assessed." *In Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93 (2016), the Supreme Court held that § 284 "contains no explicit limit or condition" on when a district court may award enhanced damages, but instead allows courts to "punish the full range of culpable behavior." *Id.* at 103, 106. This "sort of conduct warranting enhanced damages has been

variously described in our cases as willful, wanton, malicious, bad-faith, deliberate, consciously wrongful, flagrant, or—indeed—characteristic of a pirate." *Id.* at 103–04. Thus, under *Halo*, willfulness is not a prerequisite to awarding enhanced damages, nor are enhanced damages required upon a finding of willfulness. *See id.*; *id.* at 106 ("none of this is to say that enhanced damages must follow a finding of egregious misconduct"). Instead, "courts should continue to take into account the particular circumstances of each case." *Id.* However, enhanced damages are generally reserved for "egregious cases of misconduct beyond typical infringement," such as those "typified by willful misconduct." *Id.* at 106, 110. To the extent that enhanced damages are based at least in part on willfulness, "[k]nowledge of the patent alleged to be willfully infringed continues to be a prerequisite to enhanced damages." *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1341 (Fed. Cir. 2016) (citing *Halo*, 579 U.S. at 104)); *see also Finjan, Inc. v. Cisco Sys. Inc.*, 2017 WL 2462423, at *5 (N.D. Cal. June 7, 2017).

Intel argues that "VLSI has offered no evidence that Intel's conduct came even remotely close to meeting that heightened standard" but instead that "the record shows nothing more than a 'garden-variety hard-fought patent case' in which Intel has advanced non-frivolous defenses." Intel Mot. at 24 (citing *Presidio Components, Inc. v. Am. Tech. Ceramics Corp.*, 875 F.3d 1369, 1382–83 (Fed. Cir. 2017)). In response, VLSI puts forth its evidence of willful infringement (addressed above by the Court), but does not put forth any evidence of egregious conduct. VLSI Opp. at 24–25.

The Court agrees with Intel. As discussed above, the Court has found as a matter of law that VLSI cannot prove that Intel willfully infringed the Asserted Patents. Furthermore, VLSI puts forth no facts sufficient to show, and thus cannot prove as a matter of law, that Intel engaged in egregious conduct based on Intel's conduct up to this point. Intel's Motion for Summary Judgment of no enhanced damages is granted. If applicable, VLSI may reassert its claim of egregious conduct supported by evidence relating to conduct occurring after VLSI filed its Motion for Summary Judgment.

IV. ORDER

For the foregoing reasons, IT IS HEREBY ORDERED that:

1. VLSI's Motion for Summary Judgment that Intel is barred under res judicata and collateral estoppel from making its license defense is DENIED. The Court will issue a supplemental order that addresses the parties' remaining license defense arguments.
2. VLSI's Motion for Summary Judgment that Intel is estopped from using four obviousness combinations – (2) Rakshani and Willingham; (3) Rakshani and Khellah; (4) Okada, Zakel, and the Lee Book; and (6) Pahl, Shibata, and Basol – is GRANTED; it is DENIED as to (1) Nehalem, Gunther, and Willingham and (5) Okada, the Lee Book, and the Intel P1264 Package Process. The challenge to the Lee Book and AAPA is not properly before the Court and thus there is no ruling on it.
3. Intel's Motion for Summary Judgment that it does not literally infringe the '836 Patent because it does not meet a temporal limitation is DENIED; Intel's motion that it does not infringe the '836 Patent because testing is performed outside the country is GRANTED.
4. Intel's Motion for Summary Judgment that it does not infringe the '836 Patent under the doctrine of equivalents is GRANTED.
5. Intel's Motion for Summary Judgment that it does not infringe the '922 Patent is GRANTED.
6. Intel's Motion for Summary Judgment that the '922 Patent is invalid is GRANTED.
7. Intel's Motion for Summary Judgment that it does not infringe the '806 Patent is DENIED.
8. Intel's Motion for Summary Judgment that its manufacturing processes do not infringe the '672 Patent is DENIED.
9. Intel's Motion for Summary Judgment that it did not willfully or indirectly infringe the Asserted Patents is GRANTED.
10. Intel's Motion for Summary Judgment for no enhanced damages is GRANTED without prejudice to reasserting a claim based on evidence postdating the filing of VLSI's opposition to this motion.

Dated: December 7, 2023

BETH LABSON FREEMAN
United States District Judge